INVITED PAPER

Enabling Scalable Hybrid Systems: Architectures for Exploiting Large-Area Electronics in Applications

To explore platform architectures along with the supporting circuits and devices, we consider a self-powered sheet for high-resolution structural health monitoring.

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ABSTRACT | By enabling diverse and large-scale transducers, large-area electronics raises the potential for electronic systems to interact much more extensively with the physical world than is possible today. This can substantially expand the scope of applications, both in number and in value. But first, translation into applications requires a base of system functions (instrumentation, computation, power management, communication). These cannot be realized on the desired scale by large-area electronics alone. It is necessary to combine large-area electronics with high-performance, high-efficiency technologies, such as crystalline silicon CMOS, within *hybrid systems*. Scalable hybrid systems require rethinking the subsystem architectures from the start by considering how the technologies should be interfaced, on both a functional and physical level. To explore platform architectures along with the supporting circuits and devices, we consider, as an application driver, a self-powered sheet for high-resolution structural health monitoring (of bridges and buildings). Top-down evaluation of design alternatives within the hybrid design space and pursuit of template architectures exposes circuit functions and device optimizations traditionally overlooked by bottom-up approaches alone.

KEYWORDS | Civil engineering computing; CMOS technology; design for environment; display devices; electric sensing devices; electromagnetic coupling; embedded systems; energy harvesting; flexible electronics; inductive power transfer; integrated circuit interconnects; internet of things; large-scale systems; power electronics; sensors; thin film devices

I. INTRODUCTION

Through five decades of Moore's-law scaling, the microchip has resulted in high-value functions, integrated both with great variety and tremendous capacity. The outcome has been an explosion of applications, continually exposing new ways in which electronics can add value. While the set of functions, and the scale with which these can be *realized*, represents enormous potential, a key aspect that now limits applications is the scale with which these functions can be *accessed*. This paper identifies *large-area electronics* (LAE) as a technology that could enable accessing of these functions on a scale and in ways that are much broader than the microchip is equipped to handle. The critical characteristic of LAE is its fabrication methods, most notably low-temperature processing. As we describe,

Manuscript received September 26, 2014; revised December 20, 2014 and January 18, 2015; accepted January 26, 2015. Date of current version May 19, 2015. Funding support for the research presented is provided in part by The National Science Foundation, through Grant ECCS-1202168 and Grant CCF-1218206, and Systems on Nanoscale Information fabriCs (SONIC), one of the six SRC STARnet Centers sponsored by MARCO and DARPA. Y. Hu and J. Sanz Robinson are supported by a Qualcomm Innovation Fellowship, and W. Rieutort-Louis is supported the Harold W. Dobbs Honorific Fellowship from Princeton. IC fabrication is provided by MOSIS.
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Digital Object Identifier: 10.1109/JPROC.2015.2399476

this raises transformational capabilities for sensing and energy harvesting. LAE is the first practical technology that can enable the formation of large numbers of transducers, which can be diverse in type, large in scale, and distributed in space (over dimensions $\sim$10 m^2). Thus, electronic functions can be coupled to physical sources of signals and energy with much greater scale and diversity than before, significantly expanding their applicability.

While the primary uses of LAE today are limited to displays and photovoltaics, research over the last ten years has resulted in a wide range of sensing/actuation and energy-harvesting technologies. These have spanned broad application spaces, involving chemical (particulate), mechanical (strain, pressure, vibration), and electromagnetic transduction. However, as this paper discusses, the challenge, when it comes to exploiting these technologies in actual applications, is that realizing practical *systems* requires combining sensing and energy harvesting with complex functions, such as instrumentation, computation, communication, and power management. LAE, on its own, cannot implement the circuits necessary for these functions on the scale required. The reason is that, while LAE circuits based on thin-film transistors (TFTs) can be formed, low-temperature processing leads to very low performance. Even with research on materials and devices yielding substantial enhancements in performance and manufacturability, the speed and energy efficiency of the TFTs remain orders of magnitude below those of the transistors available in silicon CMOS, the workhorse technology used in systems today. Thus, even by standards of today, systems based on LAE alone would be highly suboptimal, limited in scalability, or both.

For this reason, there is a need to think of LAE in the context of *hybrid systems*. Hybrid systems combine LAE with other technologies to efficiently and scalably enable the range of functions necessary for practical embedded systems. Such an approach seems natural given that the set of functions LAE addresses, though of high importance, is rather specific. It is important to note that the precise approaches taken to hybrid systems will have broad implications on the range of applications that can ultimately be addressed, the scale with which respective functions (and thus overall systems) can be realized, the viability of systems in terms high-volume manufacturing, and the technology roadmap necessary for sustained progression of systems. Thus, this paper explores hybrid approaches, by starting with the following questions.

1) **What technologies provide the appropriate synergies?** A variety of technologies bring strengths that are complementary. Though a multitude of technologies might eventually play a role, the design and manufacturing methodologies and infrastructure are likely to increase in complexity with the number of technologies involved. For the initial viability and long-term sustainability of hybrid systems, reduction to a small number of technologies is likely necessary. The factors to consider include manufacturability, efficiency for realizing the range of core functions, achievable form factors, etc. To approach the next questions quantitatively, the later sections of this paper focus on silicon CMOS as a complimentary technology. We find that it can adeptly address the range of technical needs envisioned within hybrid systems.
2) **What platform architectures enable the technologies to be leveraged *jointly* in a manner that is *scalable?*** A hybrid approach gives us the benefit that the various strengths of different technologies can be leveraged. However, system architectures are required that are integrative, exploiting the technological strengths jointly, yet without adversely constricting the respective design spaces. As we describe, interfacing of the technologies poses a critical challenge. Using silicon CMOS with LAE as an example, we explore how architectures might be built from the start around the interfacing strategies. The interfacing strategies themselves must be generalizable, raising the need for platform architectures that can serve as templates in a broad range of applications.
3) **What circuits and devices are required to support those architectures?** The importance of the interfaces and the need for platform architectures directs us towards specific circuit functions as critical enablers for scalable hybrid architectures. This implies that circuit- and device-level optimizations can be pursued in directed ways. In addition to guiding current research efforts, this can ultimately help to establish a technology roadmap. In particular, TFTs, while unlikely to form the base for high-performance and energy-critical processing and control functions, are likely to play a critical role in enabling the interfaces. Active-matrix circuits used in large flat-panel displays today are an example of this. Looking forward to more generic sensing systems, this paper considers specific TFT circuits and optimizations in the context of interface-driven architectures for sensing, communication, and power management.

This paper is organized as follows. We next take a closer look at the technologies on which hybrid systems might be based. Then, we introduce an application case study, which serves as a driver for developing the platform architectures. From there, we explore the architectures themselves, analyzing design objectives and tradeoffs on the circuit and device levels.

II. TECHNOLOGIES FOR HYBRID SYSTEMS

A number of candidate technologies can be considered for realizing hybrid systems. The actual materials that can be

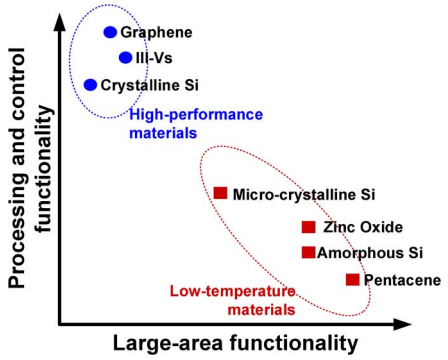


Fig. 1. ***Some candidate technologies (based on high-performance and low-temperature materials) for consideration in hybrid systems.***

used are determined by the various system attributes we aim to achieve. The sections that follow first consider various materials options in the context of these system attributes and then direct the focus to two particular technologies for detailed further study.

A. Large-Area Versus Processing and Control Functions

Fig. 1 considers two abstract dimensions corresponding to the primary system attributes of interest: 1) large-area functions and 2) processing and control functions. Processing and control functions correspond to the underlying functions necessary for enabling systems (instrumentation, computation, power management, communication), while large-area functions correspond primarily to sensing, energy harvesting, etc., which enabling interfacing with physical sources of signals and energy. However, in the context of hybrid systems, large-area functions must also encompass *scalable interfacing* of the large-area sensing and energy-harvesting functions with the underlying processing and control functions. As already mentioned, an example of this is the TFTs used in flat-panel displays for active-matrix and scanning circuits in order to reduce the signals between large-area pixel arrays and pixel-driver electronics. A critical challenge is that generalized sensing applications will raise far more diverse needs in terms of interfacing.

With regards to large-area functions, system components can be realized by either directly depositing desired materials and devices on an eventual substrate (this can include deposition on a secondary substrate that is integrated via lamination) or by transferring desired materials and devices from a fabrication substrate to the eventual substrate. Generally speaking, scalability, particularly over large areas, makes transfer from smaller substrates unattractive due to the many individual transfer steps that would typically be required. On the other hand, direct deposition on large substrates (several m^2) requires low-temperature processing. Reasons for this include temperature limitations of typical large-area processing equipment ($\sim$300 °C), temperature limitations of large-area substrates such as plastics ($\sim$200 °C), stresses due to differential thermal expansion of materials over large areas, etc. Thus, we assume that large-area functions will generally involve low-temperature materials.

The need for large-area functions to address diverse interfacing within hybrid systems necessitate a broad range of circuit functions, which require devices such as transistors, diodes, etc. Some prominent semiconductor materials for forming low-temperature TFTs are identified in Fig. 1. Table 1 provides a brief survey of these. A range in materials properties is observed, leading to a range in achievable TFT performance, manufacturability, etc. Since the expected electrical performances are all substantially lower than those of technologies considered as follows for processing and control functions, the broad architectural decisions driving hybrid-system design are not strongly impacted. However, the importance of interfacing functions (as highlighted in the rest of this paper), means the potential applications that can be addressed are strongly impacted, making the interfacing technology an important system consideration.

Table 1 Survey of TFT Technologies Compatible With Low-Temperature Processing, Thus Enabling Interfacing With Large-Area Functions

TFT Semiconductor	Substrate material	Process Temp.	Bi-/uni-polar	Field effect mobility	Manufac-turability	Ref.
Microcrystalline silicon	Polyimide	250°C*	Bipolar	n:300 cm^2/Vs p:150 cm^2/Vs	High cost laser crystallization	[1]
Amorphous silicon	Polyimide	150°-250°C	Unipolar (n)	1.0 cm^2/Vs	Established industrial technology	[2,3]
Pentacene	Polyimide, Polyethylene terephthalate/ naphthalate	<100°C	Unipolar (p)	1.0 cm^2/Vs	Degradation in atmosphere	[6,7, 9]
ZnO	Polyimide	200°C	Unipolar (n)	20 cm^2/Vs	Atomic layer deposition	[6,9]

*with thermal barrier

Table 2 Comparison Between a-Si TFTs and Crystalline-Silicon CMOS Transistors (130 nm)

	a-Si TFT	c-Si CMOS (130nm)
Mobility (μ_e/μ_h)	μ_e: 1 cm^2/Vs μ_h: 0.05 cm^2/Vs	μ_e: 1000 cm^2/Vs μ_h: 500 cm^2/Vs
$t_{dielectric}$	280nm	2.2nm
V_{DD}	6V	1.2 V
$C_{GD}/_{GS}$	3.3 fF/μm	0.34 fF/μm
f_T	1MHz	150 GHz

With regards to processing and control functions, having addressed scalability over large areas for the sensing/energy-harvesting and interfacing functions, high-performance materials rather than low-temperature materials can now be considered. Further, the resulting high-performance devices can correspond to a large proportion of the sensing and interfacing functions within a system, necessitating fewer such devices and possibly making a range of assembly and/or integration approaches viable (e.g., transferring). Fig. 1 identifies several high-performance semiconductor materials. Indeed, some of these correspond to thin-film technologies, which can potentially benefit the overall system form factors achievable. Examples include single-crystalline silicon [10], III–V's [11], graphene [12], etc., all achievable by transferring entire devices or circuits.

B. Amorphous Silicon and Silicon CMOS for Hybrid Systems

To explore hybrid-system architectures, in this paper we focus on amorphous silicon (a-Si) as a representative technology for large-area interfacing functions, and we focus on crystalline silicon CMOS as a representative technology for processing and control functions. A-Si is chosen because it offers the benefits of relative maturity, making experimentation at the system level possible, and commercial prominence to date (in flat-panel display applications), providing possible paths and models for large-scale manufacturing. Similarly, silicon CMOS is chosen because it offers the benefits of accessibility on large scale and, in addition to being a high-performance material, continued compatibility with nanoscale lithography. As a result, it is able to address processing and control functions at increasingly high-performance design points, displacing less accessible technologies that have previously been required (e.g., III–V's).

To emphasize, more quantitatively, the divergent characteristics of the two technologies, Table 2 summarizes key aspects of the transistors. For a-Si TFTs, low-temperature processing results in reduced field-effect mobility, degraded gate-stack scalability, and the need for increased channel-overlap margin (due to the expansion and contraction of thin-films during processing), leading to higher device capacitances [13], [14]. The net result is an order of magnitude higher supply voltage and five orders of magnitude lower unity current-gain frequency f_T. This directly translates to lower circuit efficiency and capacity for implementing system functions. Thus, the optimal design point for hybrid architectures will emphasize CMOS for implementing the energy- and performance-critical blocks.

Before proceeding to the specific subsystem architectures, Table 3 provides a high-level view of how the technologies will be utilized, based on the respective strengths they bring to various system functions. As shown, on the highest level, the technologies play highly complementary roles (except for computational functions, where CMOS dominates LAE). The focus of the remaining paper is to

Table 3 High-Level View of the Complementary Strengths of the System Technology and the LAE Technology Towards System Functions

	CMOS ICs	Large-area electronics
Sensing	+ Precision instrumentation	+ Diverse transducers, large substrates
Power management	+ (Dynamic) control, DC/DC conversion, regulation	+ Large-dimensioned energy harvesters
Communication	+ Physical-layer transceivers (wired/wireless)	+ Low-loss interconnect for 1cm-10m telemetry + Large-dimensioned antennas
Computation	+ >1B high-performance logic gates	- Low-performance/density/efficiency devices

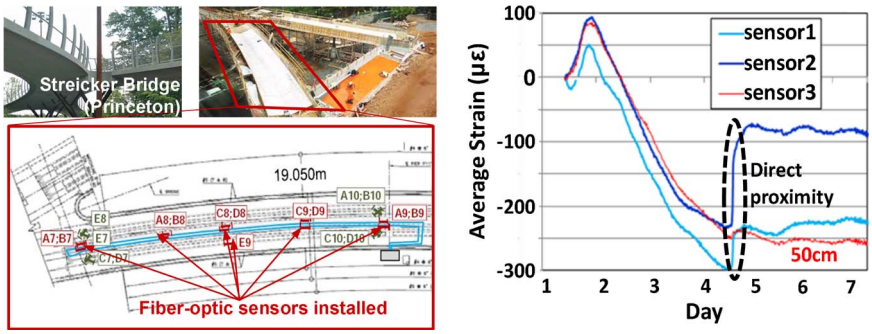


Fig. 2. ***Streicker Bridge (Princeton University) has been instrumented with fiber-optic strain sensors at the locations shown (left). During a particular week the bridge experienced a crack, causing sensors in close proximity to exhibit large change in strain signal (right).***

explore architectures that enable these capabilities to be leveraged jointly and scalably within systems without constricting the respective strengths of each technology.

III. APPLICATION DRIVER: STRUCTURAL HEALTH MONITORING

To expose the challenges facing hybrid system design and to develop the platform architectures required, we focus on an application driver. The application is structural health monitoring (SHM) of critical civil infrastructure, such as bridges and buildings. SHM can enable early-stage detection of structural degradations, mitigating hazards and providing decision support for directing maintenance efforts and investments [15]. Recent reports suggest that over 150 000 bridges in the U.S. are structurally deficient or functionally obsolete [16], making effective and broadly applicable SHM of critical importance.

Several sensing approaches have emerged to address SHM (modal analysis [17], piezoelectric sensors [18], acoustic monitoring [19], etc.). Unfortunately, these have all been limited in their ability to provide reliable and relevant information because they take an *indirect* approach to damage detection. The underlying variable of importance is mechanical stress, which is the primary determinant of when materials fail. However, stress cannot be measured directly through practical modalities. Strain, on the other hand, is a first-class indicator of stress. The challenge with measuring strain is that sensing must be performed in close proximity to damage. As an example, Fig. 2 shows strain measurements from a footbridge on the Princeton University campus. We instrumented the bridge with fiber-optic strain sensors (at the locations shown) during pouring of the concrete. The data shown is from three sensors during a particular week when the bridge experienced a crack (~0.1 mm opening), which, though benign, would be of interest for long-term risk and maintenance assessments. We see that Sensors 1 and 2, which are in the immediate proximity of the crack or intersect the crack, show large changes in strain. However, Sensor 3, which is just 50 cm away from the crack, shows no discernible change in strain. Under the practical but relatively controlled monitoring conditions, the uncertainty of the monitoring system is roughly four microstrain ($\mu\varepsilon$); nonetheless, the data shows that proximity sensing can provide robust monitoring even with substantially higher uncertainty (by well over an order of magnitude). Detailed short-term evaluation of short-gauge resistive sensors, which are considered later in this paper, and their behavior for SHM in proximity-sensing scenarios is provided in [20]. This study suggests that important parameters pertaining to damage (location, spatial extent) can be accurately inferred, with sensor measurements showing ~31 $\mu\varepsilon$ uncertainty in the tests. Thus, we see that such an approach is promising under practical on-site conditions; but, there is the need for strain measurements to be taken with high density (centimeter-scale), implying the need for *very large scale sensing* to address regions of relevant size in a structure.

Beyond short-term uncertainty of sensing, reliable long-term monitoring faces additional concerns: notably, the reliability of sensor installation and the stability of the sensors. Details pertaining to these are not yet known, with research on going, particularly for the sensing technology considered in this paper. Nonetheless, previous studies provide insights. For instance, with respect to installation, resistive strain-gauges employing a similar substrate (polyimide) show successful installation and operation on three bridges over periods exceeding 12 years [21]. Studies of other sensors (fiber optic), having a similar substrate [22] and using similar adhesives for bonding [23], show similar long-term performance. With respect to stability, resistive strain gauges have been measured to have drift on the order of 1 $\mu\varepsilon$/year [21], which is well below that required for damage detection [20] and dynamic monitoring [24] and can also be negated using a stable reference (such as fiber-optic sensor based on Bragg-gratings [21]). Further, to address temperature stability several successful approaches have been explored (e.g., [21] and [22]). Thus, while a number of important aspects remain to be investigated, a

technology that enables dense strain sensing over large regions opens up promising possibilities to address the challenges faced in SHM.

The following sections explore the technology and architectures through which hybrid systems achieve this. In addition to large scale sensing, there is also the need for self powering, so that the system can provide persistent and autonomous monitoring, as well as communication, both so that data acquired over a large number of sensors can be aggregated and so that the aggregated data can be relayed to centralized points for analysis. A remaining capability of importance is embedded data analysis for extracting key features and/or instances from the sensed data in order to reduce communication costs. The architectures presented make it possible to readily incorporate local computation. However, computational functions are likely to be implemented in CMOS, as conventionally done today. Given our focus on hybrid architectures, we thus omit discussion of the computational subsystem.

IV. HYBRID ARCHITECTURES AND CIRCUITS

This section looks, quantitatively, at hybrid architectures for the key subsystems. In particular, this implies architectures that attempt to optimally distribute functionality between LAE and CMOS. As mentioned, the distinct challenge this raises is the interfacing now required between the technologies. Thus, specialized circuit considerations and circuit topologies, which do not arise in the context of conventional architectures, are necessary.

Focusing on the application case study from Section III, Fig. 3 shows the system architecture for a self-powered, high-resolution strain-sensing sheet for SHM [25]. The distribution of functionality for the various subsystems is summarized. Each technology enables scalability of its respective component functions. However, the subsystem architectures integrating the component functions require optimization across the technology boundaries. These optimizations are performed at the level of a subarray, which consists of subsystems for sensing, power management, and communication. System scalability is then achieved by replicating the subarray over the large-area sheet. In a typical SHM application, a large number of subarrays may be required. Currently, no high-volume process exists for electrically interfacing small CMOS die to large ($\sim$10 m^2), flexible sheets. Single-chip assembly processes have been established for interfacing CMOS ICs to LAE via conductive bonds [26]. Indeed, these are employed successfully in flat-panel display applications, where TFT backplanes are integrated with CMOS driver ICs. However, large-scale sensing applications, where we envision interfacing with a large number of CMOS die, are unlikely to be addressed by single-chip assembly approaches, particularly where the robustness of the bonds is compromised due to large-area and flexible substrates.

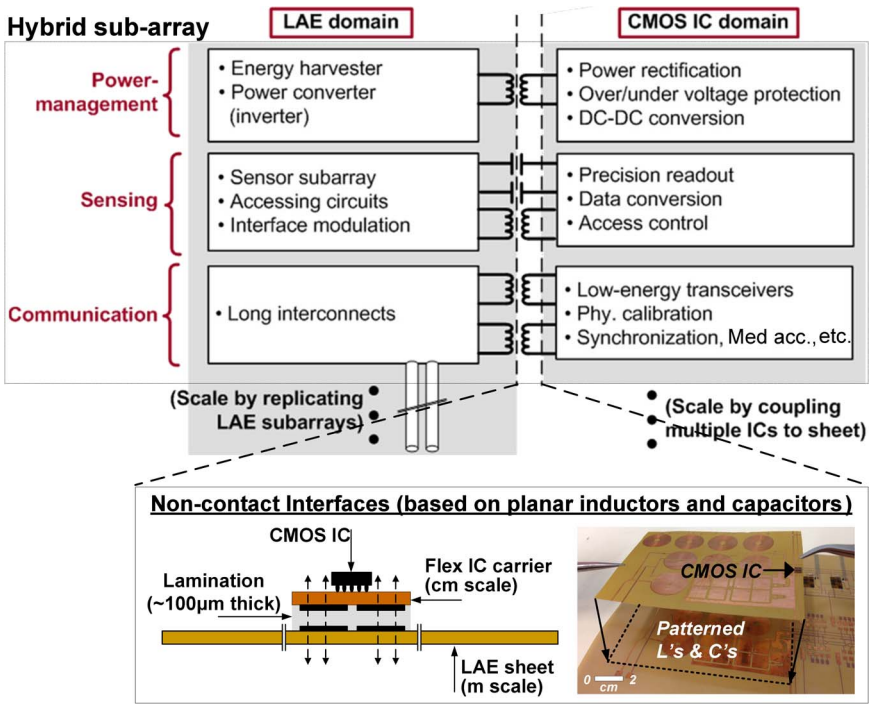


Fig. 3. *System architecture of hybrid strain-sensing sheet for SHM, based on noncontact interfaces between the CMOS and LAE domains.*

Table 4 Characteristics of Capacitive and Inductive Interfaces Employed in the Hybrid System

Capacitive Interfaces	Inductive Interfaces
• High capacitance density (~100pF/cm^2)	• Robust to proximity, alignment variations
• Frequency independ ent efficiency due to low loss mechanisms (R_{IF})	• Frequency dependent efficiency due to loss mechanisms ($R_{1/2}$)
• Voltage signals incur attenuation due to capacitive voltage division	• Voltage (current) signals can be stepped up through turns ratio

Focusing on the need for a high level of system scalability, the SHM system described employs noncontact interfaces based on inductive and capacitive coupling. As shown in the figure inset, the CMOS die are bonded to a credit-card sized flexible carrier (similar to high-volume assembly available today for RFID cards [27], [28]), and planar coupling inductors and capacitors are patterned on both the flexible carrier and the large-area sheet. System assembly is then achieved through low-cost sheet lamination of many CMOS carriers to the large-area sheet. Experimentally, lamination is achieved with adhesive thickness $< 100\ \mu$m, making efficient proximity coupling possible with the patterned capacitors and inductors.

The resulting interfaces now enable functionality to be optimally distributed between the two technology domains. However, the interfaces also raise important challenges and opportunities that become primary drivers for architectural design. A notable challenge, apparent in Fig. 3, is that, compared to conventional conductive approaches, noncontact approaches require large interfaces to ensure strong electrical coupling. Typical sizes range from 1–6 cm^2. Minimizing the number of interface signals is critical for hybrid systems regardless of the interfacing strategy but is thus a primary design objective with noncontact interfacing. Before presenting further details of the subsystem architectures, we describe some key characteristics of the interfaces. These are also summarized in Table 4.

Capacitive interfaces: Patterned plates separated by lamination adhesive yield substantial capacitance, of roughly 100 pF/cm^2. Considering the small capacitive loads presented by CMOS circuits, this makes capacitive interfaces particularly attractive for transmitting signals from the LAE domain to the CMOS domain, as shown in Fig. 4. In terms of area, this implies that adequate voltage signals can be coupled with physically small interface capacitors C_{IF}. In terms of efficiency, this implies that most of the energy expended can be transferred to the load. Further, capacitors introduce negligible intrinsic loss mechanisms, such as parallel leakage resistance across the interface. Thus, efficiency has no dependence on signal frequency and can therefore accommodate low TFT speeds (though leakage mechanisms within the TFT drivers themselves may notably impact energy at low speeds).

Inductive interfaces: Inductive interfaces offer several advantages. First, inductors provide greater robustness to proximity and alignment variations compared to capacitors [29]. Second, inductors raise the possibility of voltage/current step up/down through the turns ratio of the patterned planar coils. This plays an important role for both signaling and power transfer. For signaling from the CMOS domain to the LAE domain, voltage step-up can be incorporated, enabling the low CMOS voltages (1–3 V) to be converted to the high LAE voltages typically required for adequate TFT drive current (5–30 V). For power transfer from the LAE domain to the CMOS domain, low TFT currents, which limit power handling, can be converted to high currents at the lower CMOS voltages, enabling enhanced power transfer. However, the challenge with inductive interfaces is that

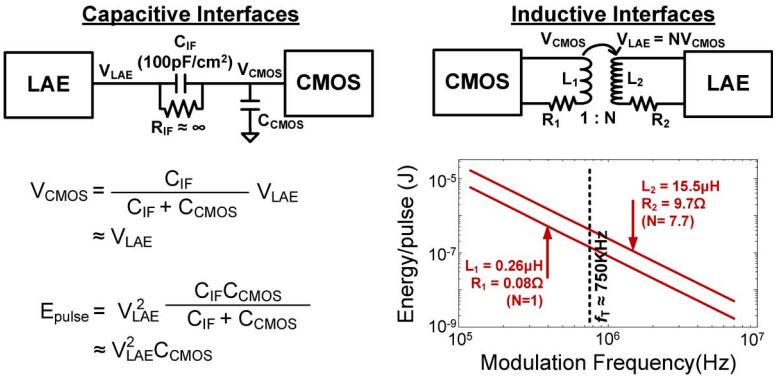


Fig. 4. ***Analysis of pulse transmission using capacitive and inductive interfaces.***

intrinsic loss mechanisms, such as series resistances, are substantial. This leads to strong frequency dependence of efficiency. The efficiency is substantially enhanced by modulating signals to the resonant frequency of the interface. The simulation in Fig. 4 considers 2 cm × 2 cm interfaces, employing typical resistances for planar coils ($L_1 = 0.26\ \mu$H, $R_1 = 0.08\ \Omega$, $L_2 = 15.5\ \mu$H, $R_2 = 9.7\ \Omega$). The energy is plotted for transmitting a modulated pulse of duration 1 ms (corresponding to typical TFT-circuit speeds) from the CMOS domain to the LAE domain. As shown, the inductive interfaces consume high energy at low modulation frequencies, with the TFT f_T noted for reference. Further, the energy cost rises, roughly cubically, with the level of voltage step up, since increasing the turns ratio results in higher voltage across the intrinsic resistance (causing quadratic energy scaling) and narrower traces, leading to higher value of the intrinsic resistance (causing roughly linear energy scaling) [30]. Thus, to exploit the benefits offered by inductive interfaces, two critical focus areas for LAE technology optimization emerge. First is the need for high-quality metalization in order to minimize the intrinsic loss mechanisms. In the case study as follows, patterned copper traces are employed with sheet resistance of 0.5 mΩ/sq, to explore the architectural potentials enabled by inductive interfaces. Second is the need to overcome the performance limitations imposed by TFTs. In the case study, this is achieved using circuit topologies that negate the effect of performance-limiting parasitic capacitances in the thin-film devices (transistors and diodes).

The subsections that follow present the major design considerations for realizing hybrid architectures for the core system functions (sensing, power management, communication). Each subsection begins with generalized principles that follow from the basic characteristics of the two technologies and then presents how these principles are applied within architectures to implement the corresponding subsystem in the SHM sheet. As we show, the interfaces are a key driver of the architectures.

A. Architectures for Sensing

Over the past ten years, research in LAE has demonstrated the potential for realizing highly diverse sensors. Given the range of sensing devices that have been considered, specification of a generalized architecture for readout from sensor arrays is not feasible. However, commonality among many of the sensing devices can begin to be identified, providing a basis for platform architectures. In particular, many reported sensors are based on the physical responses of TFTs or materials that are integrated with TFTs to modulate their electrical behaviors. Thus, TFTs serve as transducers themselves [31] or as platforms for deriving electrical outputs from transducers [32].

Modeling sensor outputs generically as TFT currents, we can consider various options for readout architectures. We start with the question of how to partition functionality between the LAE and CMOS domains. Recent work has explored TFT circuits for instrumentation amplifiers [33]–[35] and analog-to-digital converters [36]–[39]. Though such blocks may play selective roles within specific systems, generally they exhibit substantially lower power efficiency than counterparts in CMOS, particularly when considering the effects of transistor noise.

The difference in power efficiency arises primarily due to a difference in transconductance efficiency (g_m/I_{D-S}), which is a metric for the power consumed (represented by I_{D-S}) to achieve a desired transconductance. Typically, transconductance efficiency is highest when a transistor operates in weak inversion and degrades with biasing at stronger levels of inversion. The reason for this is easily appreciated in square-law devices, where I_{D-S} increases quadratically with the gate overdrive $(V_{GS} - V_t)$, but g_m increases only linearly. Though biasing at weaker inversion is thus preferred for power efficiency, this degrades transistor speed. Namely, it reduces the absolute value of g_m, correspondingly reducing the unity current-gain frequency f_T. As discussed in Section II, the materials and device structure of CMOS transistors enables substantially higher f_T than that of TFTs. Thus, while CMOS transistors can essentially remain in weak inversion at the speeds generally required for sensor applications, TFTs must often operate at substantially stronger levels of inversion, incurring worse transconductance efficiency. For illustration, Fig. 5 shows the simulated transconductance efficiency for both an a-Si TFT and a CMOS transistor (130 nm process) versus f_T. We see that the transconductance efficiency is comparable at low f_T (only 7× lower for TFT up to ∼1 kHz), making instrumentation viable to implement in the LAE domain; however, at higher f_T's, which are still of interest for many of the applications

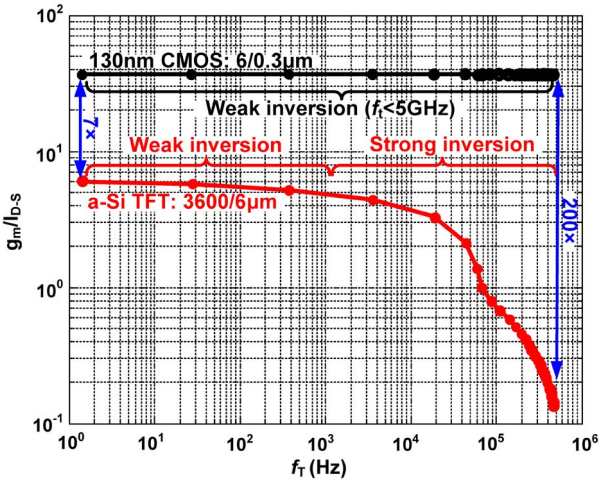


Fig. 5. *Transconductance efficiency of a-Si TFT and CMOS transistor versus f_T, showing relative degradation of TFT efficiency at higher speeds.*

envisioned, implementation in the CMOS domain becomes increasingly preferred.

To understand the impact of transistor noise, thermal and shot noise (having drain-current power spectral densities $I^2_{\text{therm}} = 4\ \text{kT}\gamma g_m$ and $I^2_{\text{shot}} = 2qn\phi_{th}g_m$, in strong and weak inversion) as well as $1/f$ noise [having drain-current power spectral density $I^2_{1/f} = K/(WLf)$] must be considered. For thermal and shot noise, input referral requires division by the transconductance squared. Thus, degraded transconductance efficiency plays a direct and significant role. As an illustration, even at arbitrarily low f_T, 1 μA biasing enables a maximum transconductance of $\sim$5 μS (versus $\sim$37 μS for CMOS), and decreases with required f_T, as shown in Fig. 5. For $1/f$ noise, the situation for TFTs is worsened by poor semiconductor and dielectric-semiconductor interface quality. While the absolute noise power spectral density may depend strongly on the processing employed, generally we see that substantially higher trap densities (and lower gate-channel capacitance C_{ox}) in TFTs leads to increased values of the process-dependent parameter K. Additionally, input referral once again involves division by the transconductance squared. As a result, TFTs exhibit substantially higher $1/f$ noise. This can be addressed to some extent by increasing the device dimensions (width W, length L). As an example, Fig. 6 shows the input-referred $1/f$ noise power spectral density, measured for a-Si TFTs and simulated for 130 nm CMOS transistors. From the data, K values of 10^{-18} A^2m^2 and 10^{-23} A^2m^2 are extracted, respectively. Much larger sizing of the TFTs lead to $1/f$ noise that is higher by just a couple of orders of magnitude. However, in practice the potential to reduce TFT $1/f$ noise in this manner is opposed by yield concerns, as reduced dielectric quality due to low-temperature processing elevates the likelihood of a shunt defect in large-dimensioned devices.

For analog-to-digital conversion, the need for mixed-signal circuits leads to dependence on both digital and analog circuits. While TFT-based ADCs limited by transistor noise have not yet been demonstrated, recent reports show that implementations limited even just by quantization noise are substantially less efficient than CMOS ADCs. A standard ADC figure of merit normalizes the energy over a conversion bandwidth by the effective resolution $FoM = P_{\text{ADC}}/(F_{\text{BW}}2^{\text{ENOB}})$ (where P_{ADC} is the ADC power, ENOB is the effective number of bits, and F_{BW} is the bandwidth of the signal being converted) [40]. Fig. 7 shows the *FoM* for recently reported TFT implementations, along with that for CMOS implementations addressing a similar application space (low-speed, low-dynamic-range sensors). With *FoMs* in the range of 10^{-9} to 10^{-6} J/conv.step [36]–[39], TFT implementations are at least five orders of magnitude less efficient than CMOS implementations [41]–[45].

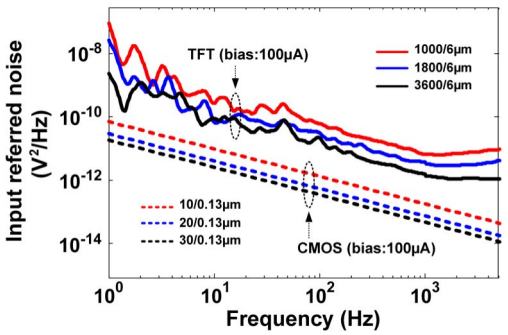


Fig. 6. *Measured (TFT) and simulated (CMOS) $1/f$ noise power-spectral densities, input referred for various sized devices with width/length values as shown (note, measured noise shown beyond 1 kHz is limited by measurement setup).*

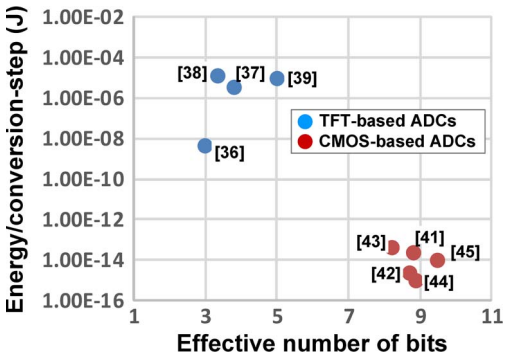


Fig. 7. *Energy per conversion step figure of merit for recently reported TFT and CMOS ADC implementations.*

Comparative evaluation of TFT and CMOS instrumentation circuits leads to the expected conclusion that in a hybrid architecture the energy- and performance-critical blocks should be delegated to the CMOS domain. However, in the context of large-area sensing, this raises an important concern. Namely, amplification and data conversion performed away from the sensors leaves readout more susceptible to extrinsic noise sources due to stray coupling. To enhance the viability of sensor arrays, particularly with large expanse, it becomes necessary to consider architectures that maximize robustness against stray coupling. In addition to shielding strategies, this drives the choice of circuit topologies. In the following, a differential architecture is presented based on synchronous readout. Differential signaling enables rejection of common-mode noise sources. Synchronous readout, as described, exploits the narrow bandwidths of typical sensor signals to effectively filter out stray sources.

Sensing Within SHM Sheet (Application Case Study): Beyond efficiency, scalability of the hybrid architectures is a key design objective. Two critical challenges are faced with regards to scalability: 1) interfacing the sensor signals to the CMOS domain through noncontact (capacitive

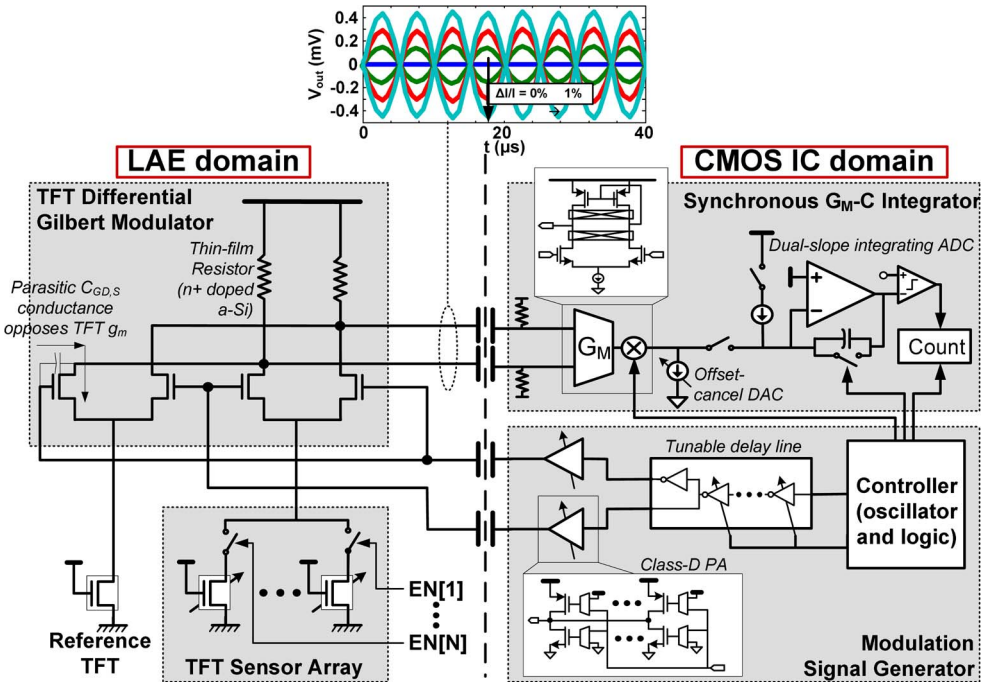


Fig. 8. ***Hybrid architecture for sensing subsystem. LAE domain consists of an array of TFT-based strain sensors and a Gilbert-multiplier for ac modulating the sensor signals. CMOS domain consists of a synchronous $G_M - C$ integrator combined with an ADC for sensor readout.***

or inductive) interfaces; and 2) enabling controlled access of individual sensors in a large array. Fig. 8 shows an architecture that addresses these challenges for the SHM system [25].

Sensor modulation for noncontact interfaces: For interfacing via noncontact coupling, the sensor signals, which are typically low bandwidth, must be modulated to an appropriate frequency. Modeling sensor outputs as TFT currents, a differential Gilbert modulator is employed, wherein the sensors provide tail-current biasing. For strain sensing, sensors are formed from a-Si TFTs, exploiting the mobility response to strain [46], [47]. A reference TFT is employed with layout orthogonal to the sensing TFTs to enable single-axis strain sensing (sensing along another axis is enabled by a second set of reference and sensing TFTs with appropriate orientation). In addition to providing common-mode noise rejection, the differential architecture has the benefit of providing first-order cancellation of large sensor-biasing currents, which would otherwise appear as an AC-modulated signal at the modulator output; as seen in Fig. 8, only the differential sensor signal is thus transmitted to the CMOS domain. The modulation signal is provided by the CMOS readout circuit. This enables synchronous readout, wherein a signal with matched phase is used in the CMOS domain (following amplification by a transconductance stage) to demodulate the sensor signal. After this, the low bandwidth of interest for the strain signals enables readout via an integrator (formed using an op-amp with feedback capacitor). Long integration periods ($> 500\ \mu s$) result in aggressive filtering of stray noise sources. Digitization is then provided by incorporating the integrator within a dual-slope ADC. For interfacing both the sensor signal and the modulation signal, capacitive coupling is employed between the LAE and CMOS domains. This is because the Gilbert modulator's frequency is limited by the f_T of the TFTs (since gate-source/-drain capacitances provide the current path shown in Fig. 8 from the input to the output, counter phase with the TFT transconductance current). Given f_T limits in the range of 1 MHz (see Table II), a modulation frequency < 100 kHz is employed, making capacitive interfaces preferred compared to inductive interfaces (as suggested in Fig. 4).

Emphasizing an approach that can be used with a broad range of sensors, the architecture in Fig. 8 focuses on TFT-based sensors. Generally, the long-term stability of such sensors can be limited by that of the TFT's electrical characteristics. In [30] a similar architecture is presented, based on AC-modulated sensor signals and synchronous readout, employing resistive strain gauges, whose long-term stability in SHM applications has been more widely studied (as described in Section III).

Sensor accessing through minimal interface signals: For individually accessing each of the sensors within the tail-biasing array, a TFT scanning circuit is developed. Active-matrix circuits have been used previously to reduce the interface signals by a square-root factor with respect to the number of sensors [48]. However, more aggressive reduction is necessary to enhance the scalability. To accomplish this, two TFT circuits are considered, requiring a total of

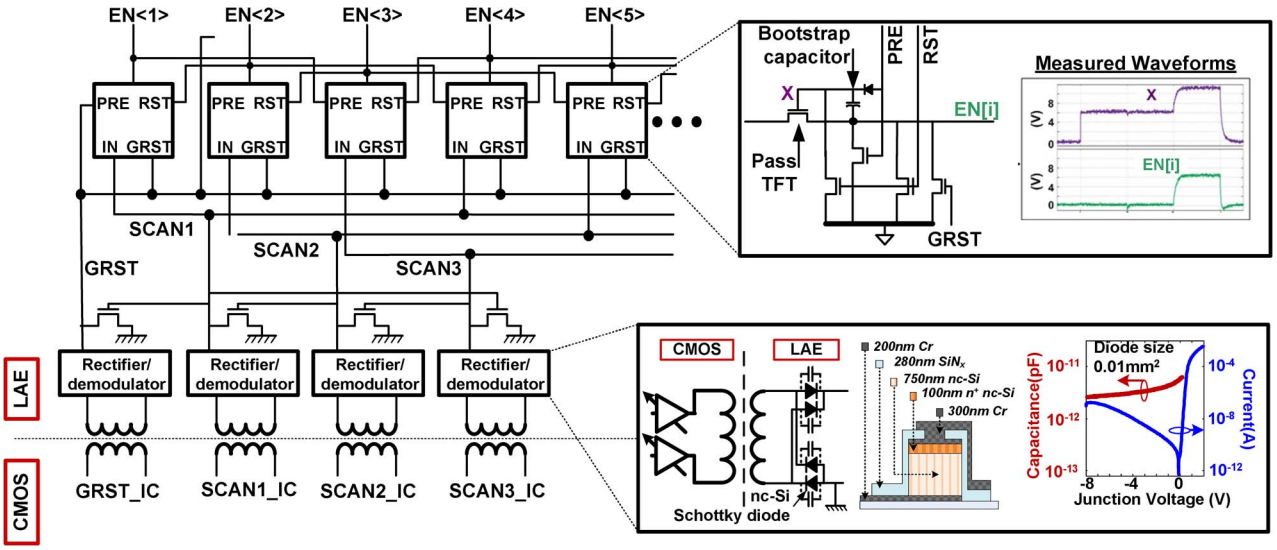


Fig. 9. ***Fully passive LAE scanning circuit for accessing individual sensors in an array. Circuit consists of inductive interfaces from the CMOS domain exploiting inductive step-up, followed by thin-film diodes for rectification and scanning elements for generating sequential enable signals EN⟨i⟩. Circuit and device details on the right illustrate measured performance.***

four and three interface signals, respectively, for accessing an arbitrary number of sensors. The first circuit is fully passive, enabling use in architectures with no power source in the LAE domain. The second circuit requires LAE powering but achieves superior efficiency, by avoiding the need for large voltage step up through the interfaces. In both cases, an important consideration for scalability is that the energy for sensor accessing should not increase with the number of sensors in the array. The circuits, described as follows, employ dynamic charge storage to ensure that power is consumed only in circuit elements involved in accessing a sensor.

Fig. 9 shows the fully passive scanning circuit [30]. A reset signal and three-phase control signals, for stepping through the sensors, are provided from the CMOS domain through inductive interfaces. Inductive voltage step up enables the signal swings required for controlling TFT access switches. The CMOS signals are modulated pulses (∼3.6 V), with a carrier frequency chosen to correspond with the resonant point of the interface; this, along with the turns ratio, enables increased signal swing. Demodulation to digital pulses is performed in the LAE domain using thin-film diodes. The resulting large-swing (∼6 V) digital pulses enable sequential activation of the scanning elements. A challenge with standard TFT technologies is the absence of complementary transistors. In particular, the availability of only NMOS TFTs in the a-Si technology would lead to signal degradation through the chain of scanning elements. To counteract this, capacitive bootstrapping is employed. This necessitates three-phase control to precharge, drive, and then reset the bootstrap capacitor in successive scanning elements.

As mentioned, losses in the inductive interfaces pose a dominant source of power consumption, particularly when generating large voltages through the inductor turns ratio. However, directed device optimization can substantially reduce power. In particular, for demodulation, thin-film Schottky barrier diodes are employed. This results in minimal voltage drop, reducing the voltage step up required. Further, hybrid nanocrystalline-/amorphous-silicon diodes are developed. These yield $> 1000\times$ higher current density compared to pure a-Si diodes [49]. As a result, smaller diodes can be employed, leading to smaller resonant capacitances for the interface. Experimentally (i.e., with the effects of parasitics considered) this results in $> 2\times$ higher carrier frequency of the control pulses, giving $> 4\times$ lower power consumption. Running at a maximum measured speed of 500 Hz, the scanning circuit consumes an energy of 286 nJ/access [25].

Fig. 10 shows the active scanning circuit [50]. Rather than relying on inductive voltage step up, this circuit employs explicit level-conversion stages following capacitive interfaces from the CMOS domain. Using two gain stages, low-voltage CMOS pulses (∼3.6 V) are converted to large-swing LAE pulses, near the LAE supply rail (∼25 V). The scanning elements consist of a resistively loaded inverting amplifier with a series output capacitor. By appropriately charging the output capacitor, using the inverting amplifier and output TFTs, logic-high and logic-low levels near the LAE supply rails can be achieved without static power consumption. In particular, eliminating static power for the logic-low state implies that all inactive elements in the chain contribute minimally to the total power. Instead, static power is consumed only in one element,

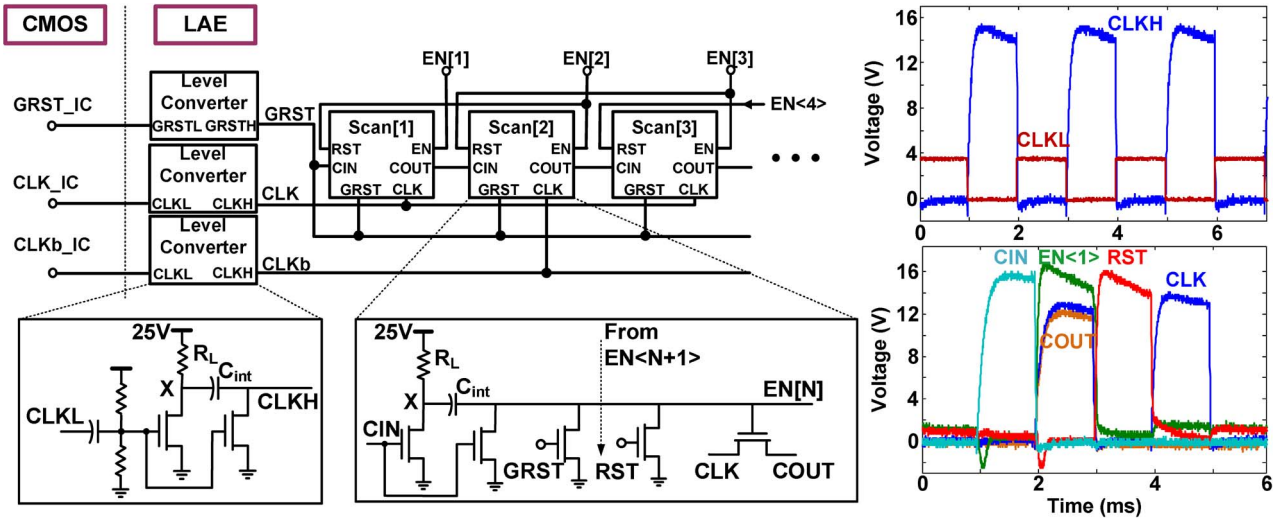


Fig. 10. *Active LAE scanning circuit for accessing individual sensors in an array. Shown on left are key circuit blocks, consisting of level converters (taking 0–3.6 V inputs from CMOS, providing 0–16 V output to LAE) and scanning elements (providing sequential assertion of EN⟨i⟩ signals). Shown on right are measured waveforms from oscilloscope capture of critical signals associated with the level converter (top) and scanning element (bottom).*

when discharging the bottom plate of the output capacitor prior to assertion of the EN[i] signal. Thus, as desired for scalability, the power consumption does not increase with the number of sensors. Running at the maximum measured speed of 10 kHz, the scanning circuit consumes an energy of 430 nJ/access. We see that the active scanning circuit enables substantially higher operational speeds and voltage swings at similar energy levels compared with the passive scanning circuit. Thus, given the prominence of the scanning circuit in the overall system, both in terms of number of TFTs required and overall energy consumed, enabling a power source and corresponding power management in the LAE domain is an important system objective.

B. Architectures for Power Management

In addition to transducers for sensing, LAE research over the past ten years has resulted in compelling transducers for energy harvesting (solar [51], [52], piezoelectric [53], [54], thermal [54], etc.). A noteworthy advantage is that LAE enables the fabrication of energy-harvesting devices that are physically large. Since the power harvested typically scales with the physical dimensions of the devices, significant power levels are possible, paving the way for fully self-powered systems of substantial scale and complexity.

A critical challenge, however, is that utilizing the harvested power effectively within systems requires power-management functions. Very limited power-management functionality has been reported in LAE aside from simple rectification and current-isolation, implemented using thin-film diodes. A primary reason for this is that typical implementations for power-management functions, based on low-current TFTs, suffer from high conduction and switching losses, thereby leading to low efficiencies. To compare the conduction and switching losses for TFTs and CMOS transistors, Fig. 11 considers various transistor sizes, on the left plotting the resistance in deep-triode mode (near zero V_{ds}) versus the total gate capacitance $(C_{g,s} + C_{g,d})$ and on the right plotting the resistance in deep-triode mode versus the gate-switching energy (assuming gate-drive voltages of 10 V and 1.2 V, respectively). With sizing having the opposite effect on conduction and switching loss (i.e., larger transistor implies lower resistance but higher switch capacitance), the difference between the TFT and CMOS curves indicates how much lower efficiency we would expect TFT implementations to be limited by.

Thus, to address the power-management functions required within hybrid systems, we are driven by two considerations. First, following the discussion of instrumentation circuits, with most loads moved to CMOS, the majority of power-management functionality can also be moved to CMOS. The architecture presented for the case study as follows emphasizes this approach. Second, for the selective functions required in the LAE domain, the use of TFTs to implement traditional topologies for power-management circuits will be highly suboptimal; however, alternate topologies can be envisioned that are a better match for exploiting LAE technology. The power inverter discussed below illustrates this.

Even with the majority of power-management functionality moved to the CMOS domain, selective functionality will inevitably be required in the LAE domain. Minimally, if we wish to exploit the energy harvesters

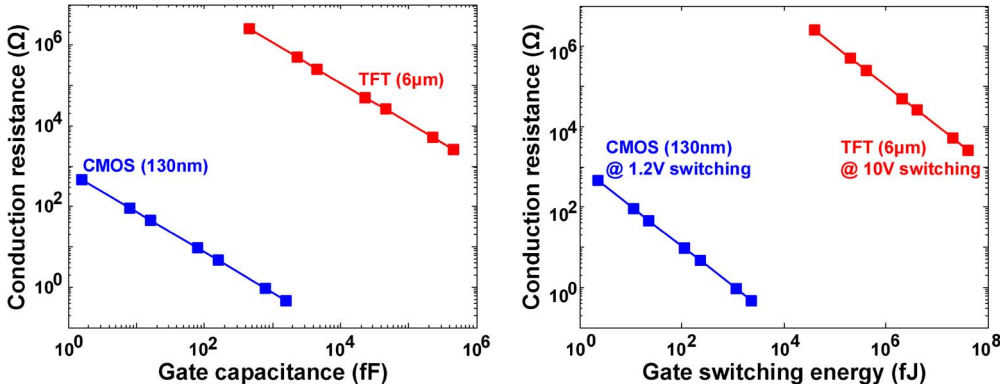
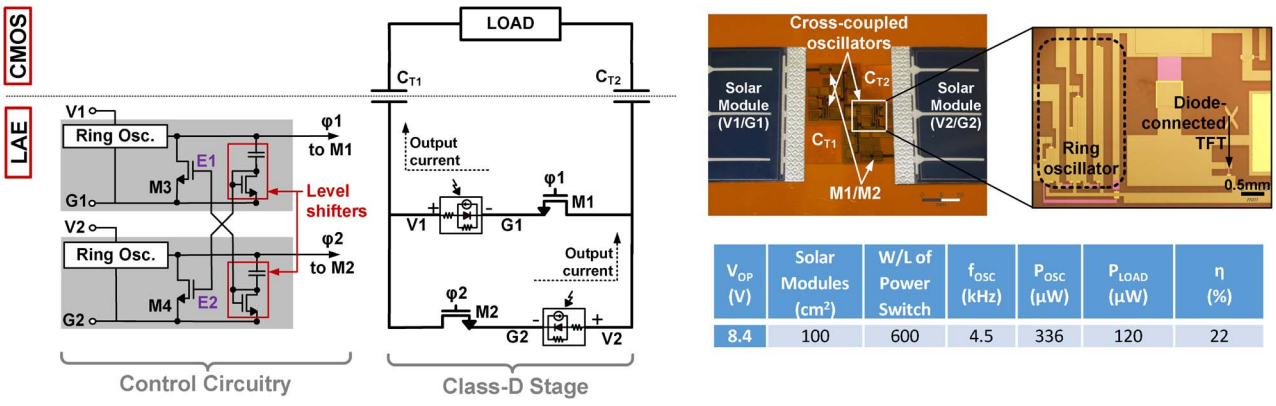


Fig. 11. *An indication of the conduction and switching losses, by considering the transistor resistance (in triode) versus gate capacitance (on left) and the transistor resistance versus gate-switching energy (on right). As seen, the conduction and switching loss values are substantially greater with TFTs compared to CMOS transistors.*

possible in LAE, power transfer to the CMOS domain is necessary. With noncontact interfaces, this implies the need for power inversion (DC-to-AC conversion). Many harvesters of interest either generate DC power directly or can readily generate DC power through rectifying diodes. Explicit conversion to AC power for transfer over inductive/capacitive interfaces imposes power losses and power-handling limitations due to the TFTs and/or other thin-film devices. To explore the challenges, we can start with the preferred topologies conventionally used for power stages. A class-D switching stage has the benefit that it can achieve very high (near 100%) efficiency. TFT implementation, however, faces several obstacles. Foremost is the absence of complementary transistors in standard TFT technologies. For instance, with only NMOS transistors available in the case of a-Si TFTs, efficient switching (i.e., with low conduction loss) cannot be achieved at high bias voltages approaching the gate voltage. Rethinking conventional switching architectures, we can arrive at the class-D topology in Fig. 12. Here, switching at high bias voltages is specifically avoided, enabling the use of only NMOS TFTs [55]. To achieve this, the topology employs two energy harvesters (solar modules in the implementation shown) that are connected with opposite polarity to the output through switching power TFTs. By generating the gate control for each TFT through circuitry powered from the corresponding energy harvester, large TFT gate overdrive is ensured, even as the absolute bias point oscillates depending on the switch states. By coupling the control circuitry through passive level-shifting stages, synchronized counter-phase switching of the TFTs is achieved, thereby generating an alternating current to the output. The challenge faced by a TFT implementation is that, typically, the control circuitry in a class-D stage



V_{OP} (V)	Solar Modules (cm^2)	W/L of Power Switch	f_{OSC} (kHz)	P_{OSC} (μW)	P_{LOAD} (μW)	η (%)
8.4	100	600	4.5	336	120	22

Fig. 12. *An all-NMOS TFT implementation of a Class-D switching power inverter. Shown on the left is the TFT Class-D power stage, consisting of solar modules with series-connected NMOS-only power switches to provide alternating output current, and control circuitry, consisting of ring oscillators synchronized vias capacitive level shifting. Shown on the right is the prototype photo with measurement summary, showing power-transfer efficiency limited to 22%.*

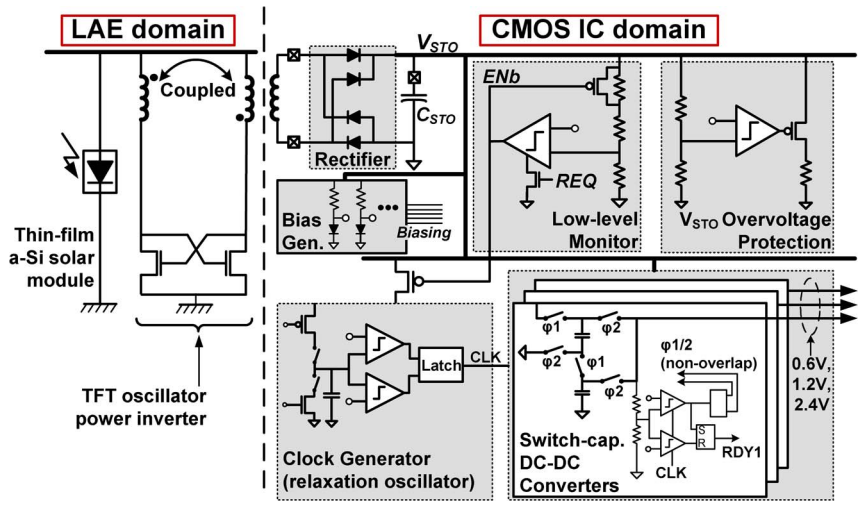


Fig. 13. *Hybrid architecture for power-management subsystem. LAE domain consists of an energy harvester (solar module), exploiting large dimensions to increase harvested power, and TFT power inverter. CMOS domain consists of power rectification, voltage regulation/conversion, and biasing circuits.*

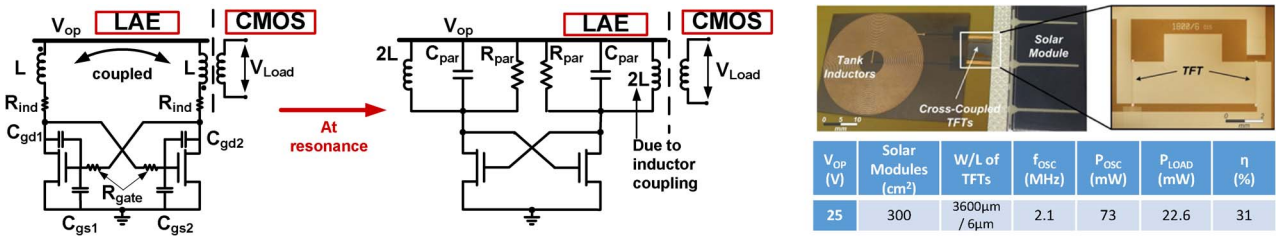
imposes minimal contribution to the power loss (since control losses do not scale directly with output power); however, even simple TFT control circuitry (based on coupled ring oscillators in the case shown) suffers substantial losses in practice. As a result, the measurements show degraded efficiency and low output power (limited by the size of power TFTs that can be driven by the control circuitry).

The case study that follows considers an alternate topology not typically employed for power inverters. A free-running *LC* oscillator is used, wherein the need for explicit control circuitry is eliminated. Further the use of inductors enables current step up during power delivery to CMOS. By thus overcoming the current limitations of TFTs and the associated control losses, ~200× higher power levels are achieved at comparable efficiency. However, as described in the following, efficient use of inductors requires overcoming the f_T limitation of the TFTs. This is achieved by exploiting the ability to form high-quality inductors in LAE, by leveraging the attribute of large area.

Power Management Within the SHM Sheet (Application Case Study): As mentioned, a key approach to the hybrid architecture is structuring the power-management functionality such that it is mostly implemented in the CMOS domain. Taking this approach, Fig. 13 shows the power-management subsystem used within the strain-sensing system [25]. For application to bridges and buildings, the energy harvester employed is a solar module. In addition to the energy harvester itself, the LAE domain consists of blocks for power inversion (to deliver power to the CMOS domain via an inductive interface) and battery management. Once AC power is received in the CMOS domain, on-chip diodes perform rectification to generate a dc voltage on a storage capacitor C_{STO}. All internal reference voltages are generated with respect to this, and the resulting voltage is maintained at operational levels by a low-level monitoring circuit (which disables the subsequent power converters when the voltage falls below 3.2 V) and an over-voltage protection circuit (which activates a low-resistance current shunting path when the voltage rises above 3.6 V). Three on-chip switch-capacitor DC-to-DC converters are then used to generate the supply voltages (0.6 V, 1.2 V 2.4 V) required by the chip. Details of the LAE blocks are discussed as follows.

Power inversion for LAE-to-CMOS power delivery: As mentioned, a conventional inverter topology (based on a switching class-D stage), when implemented using TFTs, leads to suboptimal performance. Here, the free-running *LC* oscillator shown in Fig. 14 is considered for power inversion [56]. Considering the losses imposed by the induction topology must operate at high frequencies, near or beyond the f_T of the TFTs. In fact, resonant operation of the stage has the benefit that oscillation frequency is not limited by f_T, since the TFT capacitances can be absorbed into the *LC* network, negating their effect. Rather, for correct operation, the critical concern is that the positive-feedback oscillation condition must be met. The oscillation condition represents the need for gain around a positive feedback loop at the resonant frequency [57] and can be expressed as follows for the oscillator topology shown:

$$g_m R_{par} > 1 \tag{1}$$



V_{OP} (V)	Solar Modules (cm^2)	W/L of TFTs	f_{OSC} (MHz)	P_{OSC} (mW)	P_{LOAD} (mW)	η (%)
25	300	3600μm / 6μm	2.1	73	22.6	31

Fig. 14. *LC-oscillator-based TFT power inverter [56]. Shown on the left is the power-oscillator circuit consisting of patterned planar spiral inductors resonating with the parasitic capacitances of the TFTs. Shown on the right is the prototype photo with measurement summary, showing output power greater than 70 mW at an efficiency greater than 30%.*

where g_m is the transconductance of the TFTs and R_{par} is the load resistance of each branch at resonance. Although g_m is generally low for TFTs, R_{par} can be large, even at high frequencies, if high-quality inductors are available. Exploiting the attribute of large area, large-planar inductors can be patterned, yielding high inductance, through an increased number of turns, and low resistance, through wide traces. This topology thus has the benefit of shifting the emphasis from low-quality active devices to high-quality passive devices. Incorporating the TFT and inductor parasitics shown in Fig. 14, at resonance we have

$$R_{par} \approx Q^2(R_{\text{ind}} + R_{\text{gate}}) = \frac{4\omega_{\text{res}}^2 L^2}{R_{\text{ind}} + R_{\text{gate}}} = \frac{2L}{C_{par}(R_{\text{ind}} + R_{\text{gate}})} \quad (2)$$

$$C_{par} = 2 \times (C_{gd1} + C_{gd2}) + C_{gs1,2} + C_{ox} \approx 5 \times C_{ov} + C_{ox} \quad (3)$$

where Q is the inductor quality factor, R_{ind} is the inductor resistance, R_{gate} is the TFT gate resistance, ω_{res} is the resonant frequency, L is the inductance, C_{gd} and C_{gs} are the TFT gate-drain/source capacitances (subsequently represented by C_{ov}), and C_{ox} is the TFT oxide capacitance. From this, the oscillation condition is derived to be

$$\frac{g_m}{C_{par}} \times \frac{2L}{R_{\text{ind}} + R_{\text{gate}}} > 1. \quad (4)$$

Employing typical values, g_m/C_{par} is measured to be 7.3×10^6 rad/s for a typical TFT ($W/L = 3600\ \mu\text{m}/6\ \mu\text{m}$), and Fig. 15 shows measured values of $L/(R_{\text{ind}} + R_{\text{gate}})$ for variously sized planar inductors (using low-resistance copper). We see that the oscillation condition can be robustly met.

A noteworthy point is the dependence on R_{gate}. The *LC* oscillator, as a platform circuit block, points us to a specific TFT optimization which is typically overlooked. Optimization of both the TFT layout and gate-metal is in fact crucial for making the oscillator function. While standard TFTs employ only chrome for the gate, instead deposition of a chrome-aluminum-chrome gate-metal stack enhances robustness against cracking, reducing gate sheet resistance from 10 Ω/sq to 0.6 Ω/sq in a prototype [58]. Following this, measurement of an *LC* oscillator employed as a power inverter shows nearly 200× greater output power (22.6 mW) and even higher power-transfer efficiency (31%), compared to the class-D topology.

LAE battery management: Recently, various thin-film battery technologies have emerged, addressing a critical need within energy-harvesting systems where ambient power sources are not continuously available. Though batteries can be formed over large areas, the thin-film structures result in smaller volumes and thus modest energy storage capacity. Technologies that yield high energy density are thus of interest. Commercially, "thin" (∼100 μm) lithium-ion batteries are prominent, available with energy capacities in excess of 30 J (with dimensions of ∼2.5 cm × 5 cm). An important concern with Li-ion technologies, however, is that the battery charging and discharging conditions must be regulated carefully to avoid permanent battery damage.

In particular, Fig. 16 on the left shows a typical voltage window allowed [59]. Below this, a fabricated circuit based

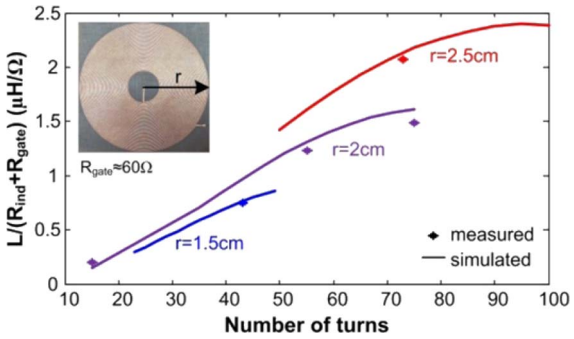


Fig. 15. *Measured inductor parameters for consideration in TFT-based LC oscillators (parameters are for low-resistance copper).*

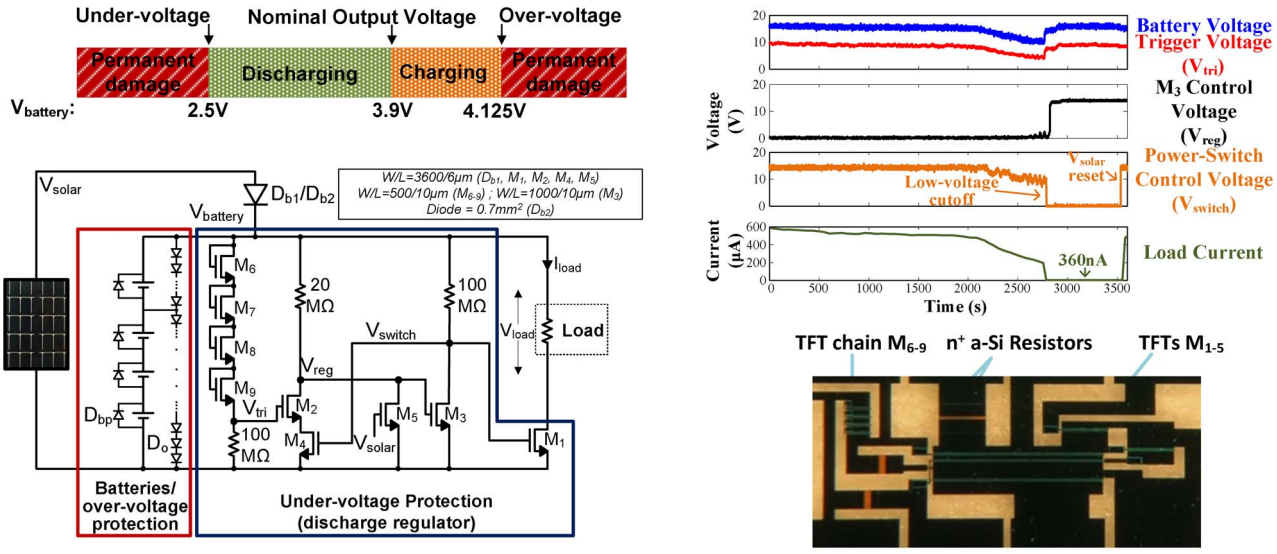


Fig. 16. ***Battery-management system for regulating charging and discharging against over-/under-voltage conditions.***

on thin-film diodes and TFTs is illustrated, providing over-/under-voltage protection. Over-voltage protection during charging is provided through shunting diodes in parallel with the thin-film battery cells. Under-voltage protection during discharging is provided by a regenerative circuit, wherein small drops in the voltage V_{tri} cause V_{reg} to rise, re-enforced by the positive-feedback path through V_{switch}. Rising V_{reg} causes V_{switch} to fall, turning off the power TFT M_1 and thereby gating the load current. Following this, the load current is re-enabled when the solar-module voltage V_{solar} is restored; this causes M_5 to reset the positive-feedback path, activating M_1. Fig. 16 on the right shows measured waveforms illustrating the operation. Namely, rapid assertion of V_{reg} can be seen, resulting in gating of the load current (to a level of 360 nA) thanks to V_{switch} control of M_1.

C. Architectures for Communication

Communication is a critical function in sensing systems. In the large-scale sensing systems envisioned, the need for communication arises in two contexts. First, since the individual sensors themselves are distributed over large areas, their data must be aggregated, both for local processing and for further communication. Second, the aggregated data must be communicated to centralized (possibly remote) base stations. Hybrid systems raise distinct opportunities in both cases.

The approach to hybrid system design illustrated in Fig. 3 optimizes the architectures across the technology domains at the level of a sensing subarray, which is composed of LAE and CMOS. System scalability is then achieved by replicating subarrays. Within the sensing subsystem (discussed in Section IV-A) data is acquired by the CMOS IC. Communication of data between the subarrays can thus be achieved by transceivers, once again in CMOS, as is preferred from the perspective of energy efficiency and performance. However, LAE raises the possibility of wired communication by enabling long interconnects over distances of 0.1–10 m between the subarrays. Avoiding the need for wireless communication, which is conventionally employed at these distances (e.g., in microsensor nodes), has substantial energy benefits by eliminating the need to radiate power via an antenna. In fact, practical demonstrations of distributed sensing applications have shown the energy of wireless communication to be a dominating factor even at low communication duty cycles [60].

On the other hand, wired communication has the potential to achieve very low energy. In the context of noncontact interfacing, the energy consists of two components considered here: 1) the energy required to transmit a pulse, by charging and discharging the interconnect capacitance $E_{\text{pulse,cap}}$ and 2) the energy required to maintain strong coupling with the interconnect for the duration of the pulse $E_{\text{pulse,couple}}$. To maintain strong coupling through noncontact interfaces, the transmitted pulse must be modulated. In particular, modulation to the resonant frequency of the interconnect network leads to large interconnect impedance, and thus substantially reduced energy for driving the pulse. The use of baseband digital pulses has been previously explored [61]. However, due to weak coupling and effective filtering over the noncontact interfaces, the robustness of pulse detection at a receiver is degraded. This necessitates large amplitudes for the transmit pulse, substantially elevating energy. In [61], a pulse height > 1 V (peak-to-peak) is employed, while the case study as follows, using modulated pulses, robustly employs amplitudes < 10 mV. For data rate r (which sets the duration of the pulse), the energy of communicating a pulse of amplitude V_{pulse} over a distance d meters can be modeled

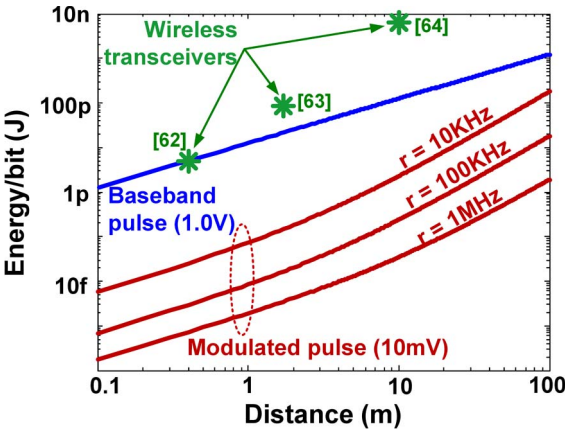


Fig. 17. *Comparison of the communication energy required with wired approaches (baseband and modulated pulses). Energy of previously reported wireless transceivers is also shown for reference.*

by considering the capacitance per meter $C_{1\,\mathrm{m}}$ and the resistance per meter $R_{1\,\mathrm{m}}$. The energy components are thus given as follows:

$$E_{\mathrm{pulse,cap}} = \frac{1}{2} V_{\mathrm{pulse}}^2 C_{1m} d \tag{5}$$

$$E_{\mathrm{pulse,couple}} = \frac{V_{\mathrm{pulse}}^2}{2Q^2 R_{1m}} \frac{1}{r} = \frac{V_{\mathrm{pulse}}^2 C_{1m} R_{1m} d^2}{2rL}. \tag{6}$$

For differential copper conductors separated by 5 mm providing forward and return current, $C_{1\,\mathrm{m}}$ and $R_{1\,\mathrm{m}}$ are measured to be 12 pF and 0.5 Ω, respectively. Assuming a typical value of $L = 3.5$ μH and $V_{\mathrm{pulse}} = 10$ mV, the total energy $E_{\mathrm{pulse}} = E_{\mathrm{pulse,cap}} + E_{\mathrm{pulse,couple}}$ is plotted in Fig. 17 with respect to communication distance. For reference, two additional energies are shown: 1) the energy for transmitting a baseband pulse of height 1.0 V, which involves only the energy component $E_{\mathrm{pulse,cap}}$; and 2) the energy of complete wireless transceivers communicating at comparable distances, based on recently reported prototypes [62]–[64]. Using the energy shown for wireless transceivers, we can see that wired communication with modulated pulses raises the potential for substantial energy reduction at the communication distances of interest. To enable such an approach to communication, the case study as follows describes the transceiver capabilities required within a hybrid architecture, namely the ability to self-calibrate the modulation frequency to the resonant frequency of an interconnect network.

Communication of data to centralized base stations will be handled primarily by CMOS, by way of wireless transceivers. An opportunity raised within hybrid systems is the use of large-area interconnect, this time for forming physically large antennas. Increased antenna dimensions result in greater radiation efficiency. In fact, recently, a radio implemented entirely using TFTs capable of communicating over distances ∼10 m has been reported [65], enabled both by the ability to form physically large antennas and the ability to generate frequencies near or beyond the f_T of the TFTs through the resonant structure described in Section IV-B1. Though such radios may be attractive in specific applications, generally CMOS radios will be preferred for greater efficiency and communication range.

Communication Within SHM Sheet (Application Case Study): Fig. 18 shows the communication subsystem used within the strain-sensing sheet. The transceivers are implemented entirely in CMOS, with LAE being used only

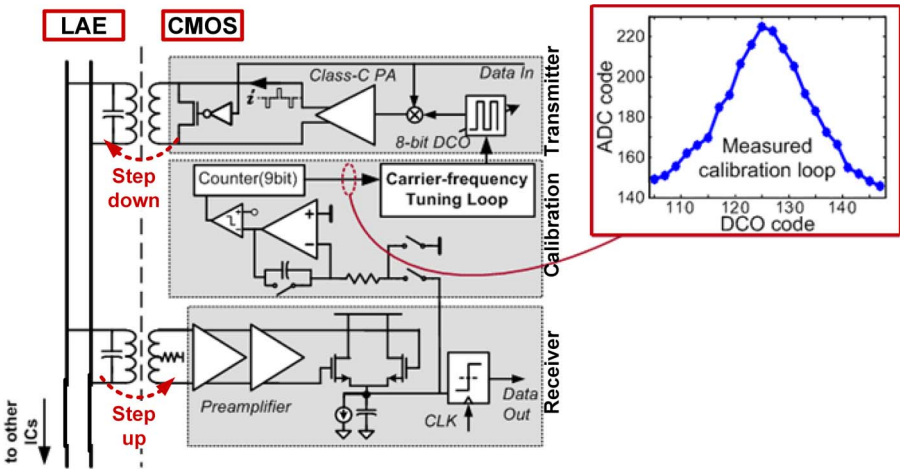


Fig. 18. *Hybrid architecture for communication subsystem. A calibration loop determines the resonant frequency of the LAE interconnects (by using the local receiver to sense the transmit amplitude), thus minimizing the drive current required by the transmitter.*

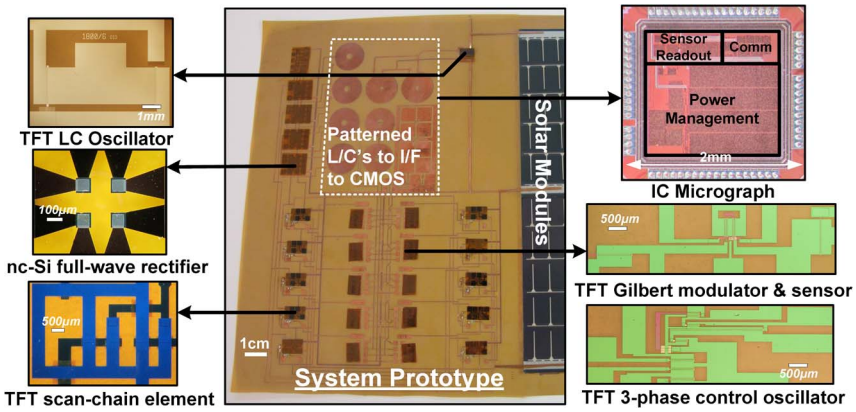


Fig. 19. ***Lab-scale prototype of hybrid LAE-CMOS sensing sheet for the SHM application case study.***

for the passive large-area interconnects. For signaling, the CMOS transceiver employs on-off keying (OOK), where the carrier frequency is selected to correspond with the interconnect network's resonant frequency, which is determined by the interface inductors and the interconnect capacitance. Generally speaking, the precise resonant frequency of the large interconnect network can be hard to predict *a priori*. As a result, the transceiver incorporates a self-calibrating architecture. During an explicit calibration phase, the transmit carrier frequency, generated using a local digitally controlled oscillator (DCO), is swept, and the resulting signal on the interconnect network is sensed using the local receiver. The peak amplitude is detected using the local receiver and used to set the DCO frequency.

The subsystem uses inductive interfaces, which enable optimization of the transmit and receive amplitudes through voltage step down and step up. In particular, since small amplitudes on the interconnect network result in reduced loss due to interconnect resistance, the transmitter employs voltage step down. On the other hand, since large amplitudes at the receiver result in increased signal-to-noise ratio, the receiver employs voltage step up. The nominal amplitudes are 20 mV for the transmit pulse and 40 mV for the receive pulse. At these levels, with a communication rate of 2 Mb/s, the transmitter consumes 13 pJ/bit (at 7.5 m communication distance) and the receiver consumes 3.3 pJ/bit. Considering the energy limit in Fig. 17 due to losses in the interconnect, we see that the initial transceiver demonstrated has potential for substantial improvement. Most notably, in the architecture of Fig. 18, although a small transmit pulse is generated, this is done via a power amplifier that incurs linear loss while operating from a 0.6 V supply. Further, limited resolution and considerable energy overhead of the DCO result in operation slightly off the interconnect resonant point with the DCO consuming roughly 5 pJ/bit of energy. Circuits optimizations in these regards can be readily envisioned and incorporated.

D. System Summary

The subsystems described previously for the SHM application case study are implemented using a custom CMOS IC fabricated in a standard 130 nm process (from IBM) and LAE samples fabricated in house, all at 180°C on 50 μm-thick flexible polyimide. A picture of the lab-scale prototype is shown in Fig. 19. Before testing this on an in-use bridge, extensive lab testing is performed. Fig. 20 shows the setups used to perform strain readout tests (left) by applying the system to a cantilever beam and communication tests (right) using serpentine interconnects also patterned on 50 μm-thick polyimide. The cantilever beam enables application of weights in a controlled manner in order to induce strain, and reference strain gauges bonded to the beam (and read out using a commercial Vishay 3800 strain-gauge reader) enable system readout validation. The serpentine interconnects provide adjustable connections, enabling communication testing over various interconnect lengths.

Fig. 21 shows measured waveforms during self-powered operation of the system, corresponding to the various subsystems. The first two waveforms show the LAE power-inverter waveform (derived from power harvested using a flexible solar module) and CMOS voltage-conversion waveforms, respectively. The next two waveforms show LAE sequential accessing of strain sensors and CMOS readout of the digitized strain measurements, respectively. Finally, the last two waveforms show communication data transmission over the LAE interconnects and CMOS recovery of digital data, respectively.

Table 5 summarizes the measured performance across all subsystems. The system performance (sensing accuracy and energy consumption) adequately address the needs of the SHM application (developed in Section III). The next

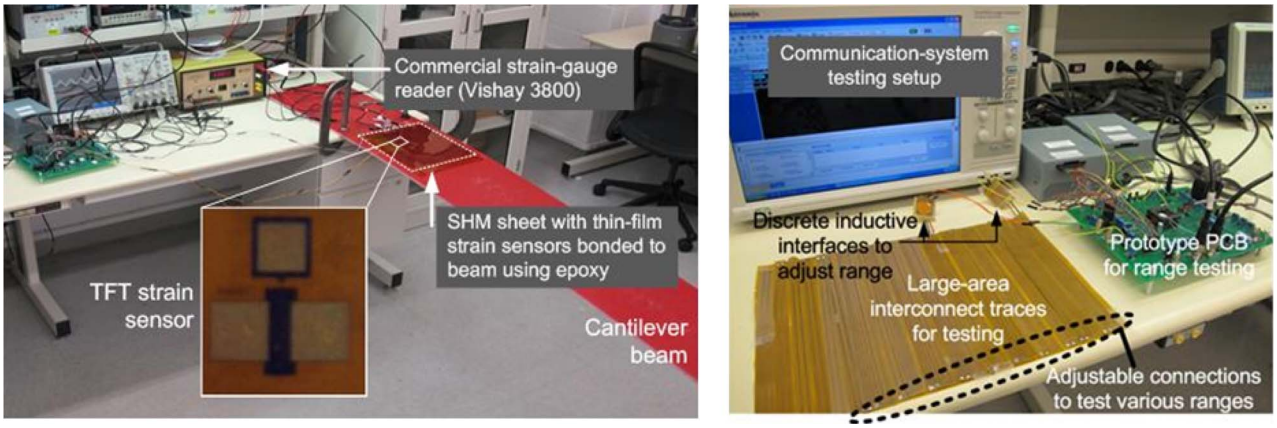


Fig. 20. *System testing setup for strain readout (left) using a cantilever beam and for communication (right) using serpentine large-area interconnects with adjustable connections for testing various interconnect lengths.*

step is to evaluate factors related to long-term stability, reliable installation, and effective data analysis. To approach this, research plans focusing on deployment of a prototype system in an in-use structure are being developed.

V. SUMMARY AND CONCLUSION

This paper takes a top-down approach to system design with large-area electronics (LAE). Starting with a particular application driver, we find that there are compelling needs that cannot be addressed by traditional technologies (e.g., silicon CMOS). By enabling large-scale and diverse sensing and energy-harvesting capabilities, LAE has the potential to address these, in turn enabling a range of high-value applications. To explore specific architectural tradeoffs and decisions, the specific application of high-resolution strain sensing for structural health monitoring is investigated. We find that for realizing practical systems of substantial scale, it is critical to introduce a technology that can efficiently enable processing and control functions, along side the sensing and energy-harvesting capabilities of LAE. This leads to hybrid systems, where, in particular we consider the use of silicon CMOS *with* LAE. The challenge with hybrid systems, however, is addressing the interfaces needed between the technologies, for the various subsystems required (sensing, power management, communication). This raises the need to think about architectures which, from the start, are built around the

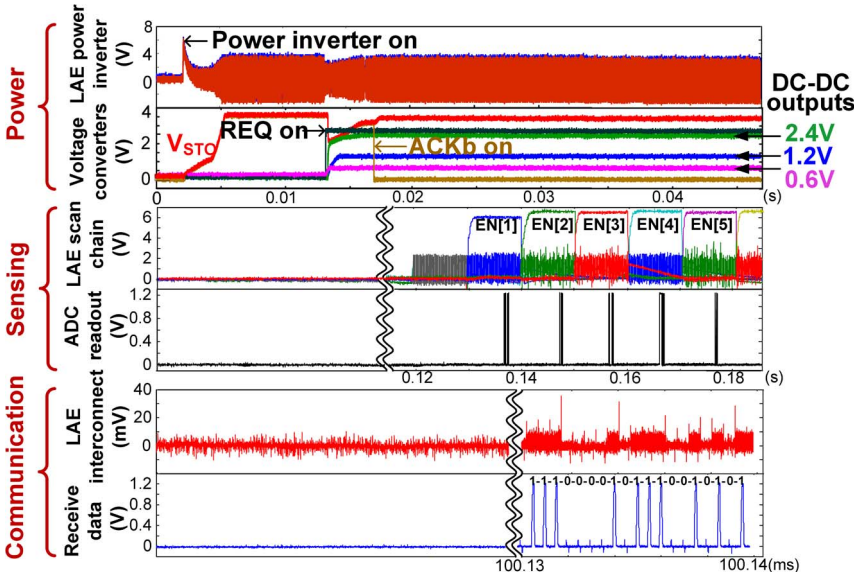


Fig. 21. *Measured waveforms showing the operation of all subsystems.*

Table 5 Measured System Performance Across the Subsystems

Performance summary			
Technology			
LAE		a-Si on 50μm polyimide @ 180 °C	
CMOS IC		130nm CMOS	
Power Management Subsystem			
TFT Power Inverter η	30%	DC-DC output voltages	0.6V,1.2V,2.4V
Solar Module Size	300cm^2	Overall DC-DC converter η	80.5%
Sensing Subsystem (for TFT sensing)			
Max. Readout Noise	22.9μStrain$_{RMS}$	Max. Readout Non-linearity	28.6μStrain
Max. Energy/meas.	434nJ	Max. Measurement/sec.	500
Communication Subsystem			
Tx Energy (@7.5m)	14.6pJ/bit	Max. Data Rate	2Mb/s
Rx Energy (@7.5m)	4.3pJ/bit	Self-calibration Loop Energy	17μJ

interfacing. Doing this points us not only to template architectures, but also to specific circuit and technological needs. Thus, optimizations can be pursed at these levels in more directed ways and with greater impact on the system level.

As an example, the use of noncontact interfaces, based on inductive and capacitive coupling, is considered. Taking this approach, this paper analyzes architectural decisions for hybrid systems, identifies platform circuits, and then explores the device optimizations that lead to enhanced system performance. Architectures for sensing, power management, and communication within the system are explored in detail: for sensing, the challenges of multisensor signal acquisition and low-noise readout from the LAE domain to the CMOS IC are addressed; for power-management, the challenges of power transfer from the LAE domain to the CMOS domain are addressed; and for communication, the challenges of low-energy data transmission among CMOS ICs on the sheet, by exploiting LAE interconnects, are addressed. While viable architectures and circuits are demonstrated, several future challenges are also envisioned. Most notably, the interface complexity is expected to increase with the number of sensors. To enable sensor scaling on a level that LAE can potentially enable, ideas that go substantially beyond active matrix and scanning-circuit approaches (wherein the number of TFTs necessary scales with the number of sensors) are needed. Additionally, low-noise sensor acquisition draws on the traditional tradeoff of noise versus bandwidth. While many applications being envisioned today require low bandwidth, the ability to acquire physical signals presenting modest bandwidth can substantially expand the application scope. Thus, we see that while there is great promise to address a range of new applications through hybrid systems, there is substantial room to innovate in a space that can, and likely must, draw on device-, circuit-, and system-level advances. ■

Acknowledgment

The authors would like to thank Y. Yao, Princeton Department of Civil and Environmental Engineering, for his support and advice on SHM based on short-gage strain-sensing arrays.

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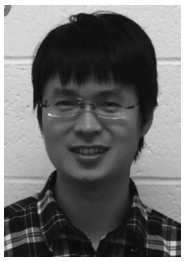


Yingzhe Hu (Student Member, IEEE) received the B.S. degrees in both physics and microelectronics from Peking University, China, and the M.A. degree in electrical engineering from Princeton University, Princeton, NJ, USA, where he is currently working toward the Ph.D. degree.

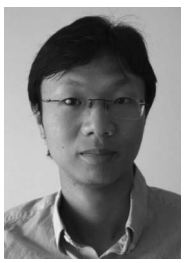
His research focuses on flexible electronics and CMOS IC hybrid sensing system design and 3-D gesture sensing system design.

Mr. Hu is the recipient of a 2013 Qualcomm Innovation Fellowship, Gordon Wu award at Princeton University, 2013 ISSCC SRP award and 2013 VLSI best student paper award.

Josue Sanz Robinson received the B.Eng. degree in electrical engineering (Hons.) from McGill University, Montreal, Canada, in 2010, and the M.A. degree in electrical engineering from Princeton University, Princeton, NJ, USA, in 2012, where he is currently working towards the Ph.D. degree.

His research focuses on developing large-area, flexible sensing systems with a "wall-paper" form factor. This has led him to research diverse aspects of system development, including novel semiconductor devices and sensors, as well as circuits and algorithms for interfacing with these sensors. Currently, he is spearheading an effort to build a large-area, flexible microphone system for speech separation. Previously, he developed high-current density, hybrid amorphous/nanocrystalline Schottky diodes and an associated low-temperature (200C) process flow.

Mr. Sanz-Robinson was a recipient of a 2013 Qualcomm Innovation Fellowship.



Liechao Huang (Student Member, IEEE) received the B.S. degree in microelectronics from Fudan University, Shanghai, China, in 2010, and the M.A. degree in electrical engineering from Princeton University, Princeton, NJ, USA, in 2012, where he is currently pursuing the Ph.D. degree.

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Mr. Huang is the recipient of a Princeton Engineering Fellowship and Gordon Wu award at Princeton University.

Tiffany Moy received the B.S.E. (*magna cum laude*) and M.A. degrees in electrical engineering from Princeton University, Princeton, NJ, USA, in 2008 and 2012, respectively, where she is currently pursuing the Ph.D. degree.

Her research interests include thin-film devices and circuits for hybrid large-area electronics/CMOS system design.

Branko Glisic received degrees in civil engineering and theoretical mathematics from the University of Belgrade, Serbia, and the Ph.D. degree from the Swiss Federal Institute of Technology, Lausanne (EPFL), Switzerland.

After eight years' experience at SMARTEC SA, Switzerland, where he was involved in numerous structural health monitoring (SHM) projects, he is now an Assistant Professor in the Department of Civil and Environmental Engineering of Princeton University, Princeton, NJ, USA. His main areas of interest are SHM methods, advanced sensors based on fiber-optics, large-area electronics and conductive polymers, SHM data management, smart structures, and heritage structures. He introduced SHM in classrooms as regular undergraduate and graduate courses at Princeton University. He is author or co-author of more than 100 published papers, short courses on SHM, and the book *Fibre Optic Methods for Structural Health Monitoring*. He is a member of the Council of ISHMII, editor-in-chief of the ISHMII's newsletter *Monitor*, member of editorial boards of ASE and SMM, voting member of ACI committee on SHM, and member of several other professional associations, including IABSE, ASCE, IABMAS, IEC, ASTM, and more.

Prof. Glisic was recipient of 2014 E. Lawrence Keyes, Jr./Emerson Electric Co. Junior Faculty Advancement Award, 2013 SHM Person of the Year Award by the editors and associate editors of *Structural Health Monitoring: An International Journal*, and along with his collaborators he won CIOB's 2013 Highly Commended Award and the First Place at the 7th Princeton Innovation Forum (2012) with their research on sensors based on large-area electronics and integrated circuits. In addition he won Princeton's E-Council 2010 Teaching Award, and he was on SEAS commendation list for outstanding teaching every year since 2011.

Sigurd Wagner (Fellow, IEEE) received the Ph.D. degree from the University of Vienna, Vienna, Austria, in 1968.

Following a postdoctoral fellowship at Ohio State University, he worked from 1970 to 1978 with the Bell Telephone Laboratories on silicon memory and chalcopyrite semiconductor solar cells. From 1978 to 1980, he organized the Photovoltaic Research Branch of the Solar Energy Research Institute (now NREL) in Golden, CO, USA, as its founding Chief. Since 1980, he has been Professor of electrical engineering at Princeton University, Princeton, NJ, USA. He introduces new electronic materials for flexible, conformably shaped and stretchable large-area displays, electronic wallpaper, electrotextiles, and electronic skin. His work ranges from the development of materials and flexible structures with fundamentally new functions to the design and fabrication of optoelectronic cells and, in collaboration with colleagues, their integration and application in systems.

Dr. Wagner is a Fellow of the American Physical Society, a corresponding member of the Austrian Academy of Science, was a Humboldt Senior Fellow in the Physics Department of the University of Konstanz, Germany, and has had research leaves at the Electrotechnical Laboratory in Ibaraki, Japan, at INESC Microsistemas e Nanotecnologias in Lisbon, Portugal, and at the Institute of Semiconductor and Solid State Physics of the University of Linz, Austria. He received the Nevill Mott Prize "for his groundbreaking research, both fundamental and applied, on amorphous semiconductors as well as chalcopyrites" in 2009, and in 2014 an ITC 10th Anniversary Prize "for his pioneering research on flexible and stretchable large-area electronics and comprehensive study on the mechanical behavior of the same, which will be applied to various products in the near future."

James C. Sturm (Fellow, IEEE) was born in Berkeley Heights, NJ, USA, in 1957. He received the B.S.E. degree in electrical engineering and engineering physics from Princeton University, Princeton, NJ, USA, in 1979, and the M.S.E.E. and Ph.D. degrees in 1981 and 1985, respectively, both from Stanford University, Stanford, CA, USA.

In 1979, he joined Intel Corporation, Santa Clara, CA, USA, as a Microprocessor Design Engineer, and in 1981 he was a Visiting Engineer at Siemens, Munich, Germany. In 1986, he joined the faculty of Princeton University, where he is currently the Stephen R. Forrest Professor in Electrical Engineering. Since 2003, has been the Founding Director of the Princeton Institute for the Science and Technology of Materials (PRISM), and from 1994 to 1995, he was a von Humboldt Fellow at the Institut fuer Halbleitertechnik at the University of Stuttgart, Stuttgart, Germany. He has worked in the fields of silicon-based heterojunctions, thin-film and flexible electronics, photovoltaics, the nano-bio interface, three-dimensional (3-D) integration, and silicon-on-insulator.

Dr. Sturm is a member of the American Physical Society and the Materials Research Society and was a National Science Foundation Presidential Young Investigator. He has won over ten awards for teaching excellence. In 1996 and 1997, he was the technical program chair and general chair of the IEEE Device Research Conference, respectively. He served on the organizing committee of IEDM (1988 to 1992 and 1998 to 1999), having chaired both the solid-state device and detectors/sensors/displays committees. He has served on the boards of directors of the Materials Research Society and the Device Research Conference, and was a co-founder of Aegis Lightwave.