A Self-Powered System for Large-Scale Strain Sensing by Combining CMOS ICs With Large-Area Electronics

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***Abstract*—We present a 2nd-generation system for high-resolution structural-health monitoring of bridges and buildings. The system combines large-area electronics (LAE) and CMOS ICs via scalable interfaces based on inductive and capacitive coupling. This enables architectures where the functional strengths of both technologies can be leveraged to enable large-scale strain sensing scalable to cm resolution yet over large-area sheets. The system consists of three subsystems: (1) a power-management subsystem, where LAE is leveraged for solar-power harvesting, and CMOS is leveraged for power conversion and regulation; (2) a sensing subsystem, where LAE is leveraged for dense strain sensing, and CMOS is leveraged for multi-sensor acquisition; and (3) a communication subsystem, where LAE is leveraged for long-range interconnects, and CMOS is leveraged for low-power transceivers. The power-management subsystem achieves 30% efficiency for DC-AC power inversion and inductive power delivery to the CMOS IC and 80.5% overall efficiency for generating three voltages via DC-DC converters. The sensing subsystem has a readout noise level of 23 $\mu\text{Strain}_{\text{RMS}}$ (141 $\mu\text{Strain}_{\text{RMS}}$ including sensor noise), at an energy/meas. of 148 nJ and 286 nJ for readout and sensor-accessing control, respectively. The communication subsystem achieves an energy/bit of 14.6 pJ/4.3 pJ (Tx/Rx) at a distance of 7.5 m and a data rate of 2 Mb/s.**

***Index Terms*—Choppers (circuits), coupled circuits, DC-AC power converters, DC-DC power converters, energy harvesting, flexible electronics, inductive power transmission, sensors, switching converters, thin-film transistors.**

I. Introduction

CMOS ICs have enabled tremendous computing, power-management, and communication capabilities for embedded sensing systems. However, a critical bottleneck is that sensing technologies have not scaled proportionately, thus limiting the level of interfacing that can be achieved between electronics and physical systems. Wireless micro-senor nodes fall short of addressing this, because their scale and density of sensing remains limited to the point of discrete nodes and because no generalized sensing technology exists that can interface with CMOS ICs in a standardized way.

Large-area electronics (LAE) is a technology wherein expansive and diverse sensors can be integrated on large (10 m^2) sheets, thus enabling sensing capabilities to scale in a manner that can match the functional capabilities of CMOS ICs. This paper presents a 2nd-generation system for large-scale strain sensing to achieve high-resolution structural-health monitoring (SHM) of bridges and buildings. In SHM, strain is a key indicator of early-stage damage [1]; however, studies have shown that strain measurements must be taken in close proximity to damage. While sensors in direct proximity to damage experience large strain (>500 μStrain [2]), sensors even a few centimeters away cannot detect the damage due to strain levels below those experienced from normal loading and environmental factors [2]. This necessitates sensing on a centimeter level, yet scalable over large portions of the structure. The presented sensing sheet incorporates the following three subsystems, which utilize LAE and CMOS ICs synergistically towards scalable architectures: 1) a sensing subsystem capable of scaling to dense, many-channel strain readout; 2) a power-management subsystem capable of enabling fully self-powered operation; and 3) a communication subsystem capable of providing low-energy data aggregation over sensing sub-arrays distributed over a large-area sheet. Compared to a previous system [3], this system incorporates several advances: including self-powered operation via embedded energy harvesting; a sensor-readout architecture that interfaces with devices capable of forming a broad range of transducers for diverse sensing applications; and fully-integrated functionality for data-acquisition, data-conversion, and calibration within the sensing and communication subsystems. The rest of the paper is organized as follows. Section I provides the system-level rationale; Section III details the architectures and circuits for the various subsystems; Section IV presents the prototype and measurement results; and Section V provides conclusions.

II. System Architecture and Rationale

Large-area electronics is a technology based on processing thin films at low temperatures. This enables the use of plastic substrates, which can be large and conformal, as well as the use of diverse materials, enabling the formation and large-scale

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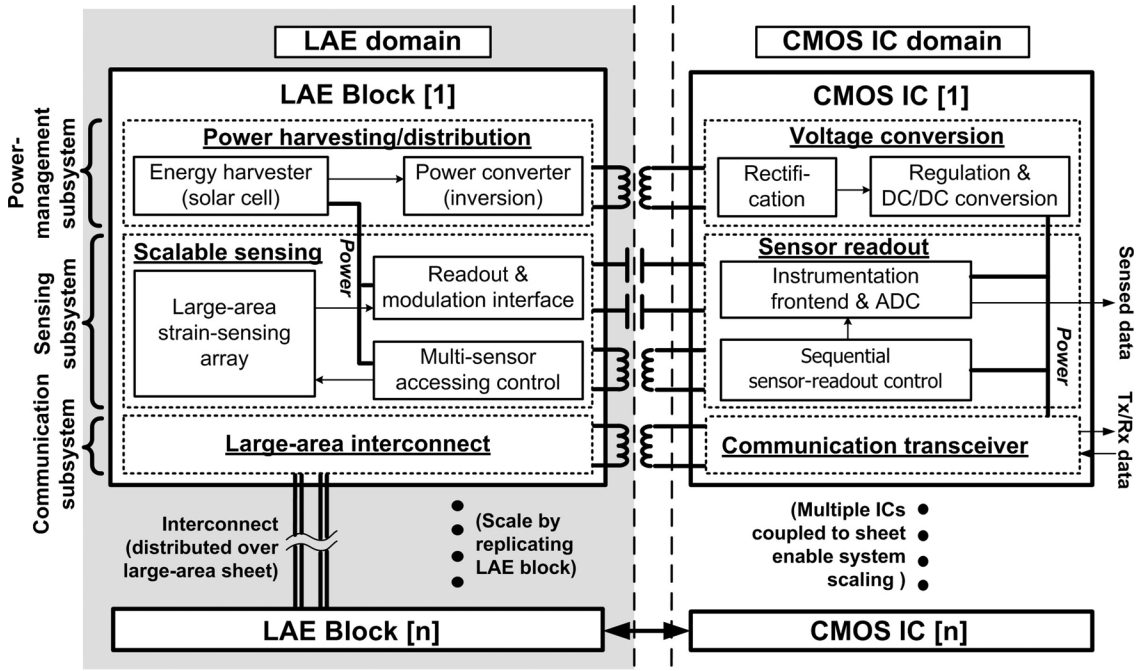


Fig. 1. Hybrid LAE-CMOS system architecture, showing functionality partitioning enabled by non-contact interfaces.

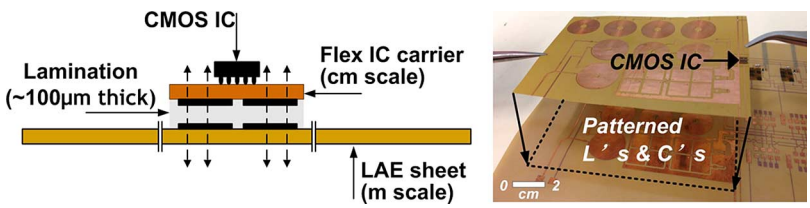


Fig. 2. Non-contact interfaces for scalable system assembly achieved via sheet lamination of a flexible IC carrier on the large-area sheet.

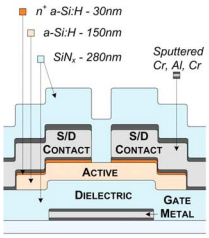
integration of a wide variety of transducers. Thin-film transistors (TFTs) are also possible and have been used to demonstrate various circuit blocks, including ADCs [4], RFID tags [5], and etc.. Various low-temperature-processed TFT technologies exist, based on semiconductors such as organics, amorphous silicon (a-Si), metal oxides, etc. In all cases, however, the performance and energy efficiency is orders-of-magnitude lower than the transistors available in CMOS ICs. CMOS thus raises much greater possibilities for realizing system functions (instrumentation, communication, power-management, computation) on a large scale, particularly in proportion to the level of sensing possible in LAE.

The objective of the proposed architecture is thus to distribute system functionality between LAE and CMOS in a manner that exploits the complementary strengths of both technologies towards scalable sensing systems. However, in combining the two technologies, the interfacing required between them now poses a critical limitation. Fig. 1 shows the architecture, wherein system scaling is achieved by replicating the LAE block and CMOS IC, and scalability of the interfaces is enabled through non-contact coupling between the technology domains. Currently, no high-volume options exist for creating a large number of metallurgical bonds from small-scale ICs to large and flexible plastic sheets. The architecture thus uses inductors and capacitors patterned on the large-area sheet and on credit-card-sized flexible IC carriers (similar to RFID assembly), as shown in Fig. 2. System assembly is then accomplished via sheet lamination. In our lab, this is performed with adhesive thickness of 100 μm; using 1–3 cm inductor/capacitor dimensions, efficient proximity coupling is thus achieved. The choice of inductive or capacitive coupling depends on various factors within the subsystems (signal frequency, voltage levels, power levels, etc.), as described in Section III.

With such interfaces, it becomes possible to selectively distribute functionality between the two technology domains for the various subsystems [6]:

Power-management subsystem. LAE enables a physically-large thin-film solar module (300 cm^2) to harvest substantial power as well as a TFT-based power inverter for DC-AC conversion of the solar-module output, permitting power coupling to the IC over an inductive interface. CMOS enables efficient circuitry for rectification, voltage regulation, and DC-DC conversion, to generate three on-chip supplies.

Sensing subsystem. LAE enables a large-area array of thin-film strain sensors as well as TFT-based control circuitry for sensor accessing and sensor-signal modulation, permitting acquisition over a capacitive interface. CMOS enables tunable instrumentation circuitry for sensor-access control, acquisition, and digitization.



	a-Si TFT	c-Si CMOS(130nm)*
Mobility (μ_e/μ_h)	2 cm^2/Vs 0.05 cm^2/Vs	1000 cm^2/Vs 500 cm^2/Vs
$t_{dielectric}$	280nm	2.2nm
V_{DD}	6V	1.2 V
$C_{GD}/_{GS}$	3.3 fF/μm	0.34 fF/μm
f_T	1MHz	150 GHz

* representative numbers are shown.

Fig. 3. Structure of the a-Si TFTs fabricated in-house and a summary of their electrical characteristics.

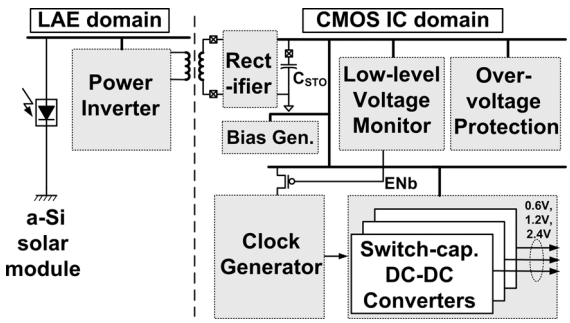


Fig. 4. Architectural blocks of the power-management subsystem.

Communication subsystem. LAE enables long-range interconnects (∼0.1–10 m) over the large-area sheet for low-energy IC-to-IC communication. CMOS enables self-calibrating digital-data transceivers [7] and, eventually, wireless communication to transmit selected data to remote servers.

Although LAE TFTs have much lower performance than CMOS transistors, the subsystems utilize TFTs to realize specific circuit functionality that is critical for enabling the architectural partitioning above. For this, we focus on a-Si TFTs, as these represent the dominant technology today, used for large-display applications [8]. Fig. 3 shows the structure of the a-Si TFTs, which we fabricate in house at 180°C on 50-μm-thick polyimide [9], along with a summary of the electrical characteristics. As shown, the performance is substantially lower than CMOS transistors, and in fact PMOS devices are not available in a standard technology due to the low hole mobility. As described in the following section, this necessitates specialized topologies for the various circuit functionality required.

III. Subsystem Architectures and Circuit Details

The following subsections describe the details of each subsystem, starting with the subsystem architecture and then the circuits in both the LAE and CMOS domains.

A. Power-Management Subsystem

Fig. 4 shows the architectural blocks of the power-management subsystem. The LAE thin-film solar module is based on the same a-Si semiconductor technology as that used for the TFTs. The DC power harvested in the LAE domain is converted to AC by a TFT power inverter and coupled to the CMOS IC via an inductive interface.

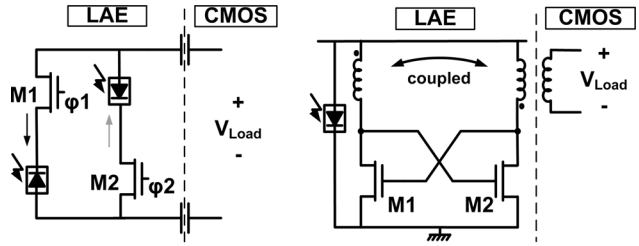


Fig. 5. TFT power inverters based on (a) Class-D topology and (b) LC-power-oscillator topology.

1) LAE Power-Management Circuits: A-Si is one of the dominant solar-cell technologies. The thin-film solar cells (also on 50-μm-thick polyimide) are capable of harvesting ∼10 mW/cm^2 under outdoor lighting conditions and ∼10 μW/cm^2 under indoor lighting conditions (consistent with typical values [10]). Adequate power for full-system operation is thus easily provided. For DC-AC power conversion, however, the TFTs pose substantial challenges due to their low currents. This implies increased conduction and switching losses, potentially degrading efficiency, as well as low power-handling capability. We previously investigated two TFT power-inverter topologies, which are shown in Fig. 5. Fig. 5(a) is a Class-D switching stage [11], which has the potential to achieve very high efficiency. In practice, however, the need for large switches M1/2 to provide adequate power, and the availability of only NMOS devices, necessitates complex synchronization control circuits, which limit both the achievable output power and efficiency. Further, the use of TFTs as switches limits the frequency to well below the TFT f_T (≈ 1 MHz), forcing the use of capacitive coupling to the IC since inductors are inefficient at the low speeds achievable. Fig. 5(b), on the other hand is a resonant LC-oscillator stage (power oscillator) [12], which can use inductive coupling. A key benefit of inductors is that only current, and not voltage, is coupled to the IC. This implies that, through the turns ratio of the coupled inductors, the large voltages used in the LAE domain can be transformed into increased current at the IC's voltage limit (3.6 V), thus elevating the power transferred.

As mentioned, however, the use of inductors requires high-frequency operation. In fact, for patterned inductors of reasonable size (1–3 cm radius), a frequency near or beyond the TFT f_T is necessary. The LC oscillator stage is able to achieve this. The inductor is formed by patterning planar spirals on the large-area sheet and the IC carrier. Forming an LC tank in this way enables the parasitic capacitances of the TFTs to be resonated out, permitting operation beyond 3 MHz, well above f_T[12]. However, for successful oscillations in the cross-coupled structure, the oscillation-condition, requiring positive-feedback gain larger than unity, must be met. The key to achieving this, despite the low transconductance of the TFTs, is the ability to pattern physically-large inductors in LAE (∼ 3 cm), which enables a high inductor quality factor Q. To see this, Fig. 6 (left), shows all of the TFT parasitics, including the gate-source/drain capacitances ($C_{gs,d}$) and gate resistance (R_{gate}) (all modeled as lumped elements since the frequencies of interest are much

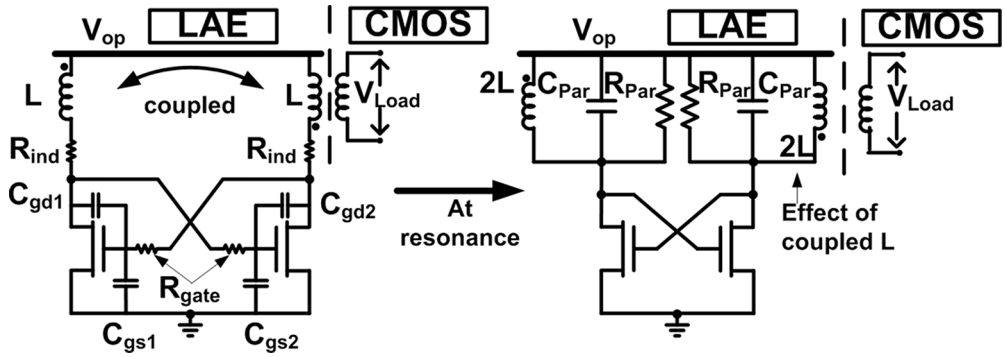


Fig. 6. LC-oscillator analysis considering the TFT parasitics.

lower than the associated time constants). It is worth noting that R_{gate} can be significant for this analysis due to the bottom-gate structure of the TFTs, which requires thin gate metallization in order to ensure reliable gate-dielectric formation [13]. At resonance, the parasitics can be represented as shown in Fig. 6 (right), where R_{Par} can be estimated by

$$R_{Par} \approx Q^2(R_{ind}+R_{gate}) = \frac{4\omega^2 L^2}{R_{ind}+R_{gate}} = \frac{2L}{C_{Par}(R_{ind}+R_{gate})} \quad (1)$$

and C_{Par} can be estimated by taking into account Miller multiplication effects:

$$C_{Par} = 2\times(C_{gd1}+C_{gd2})+C_{gs1,2}+C_{ox} \approx 5\times C_{ov}+C_{ox}. \quad (2)$$

With the TFT output resistances much larger than typical values for R_{par}, the oscillation condition thus requires that $g_m \times R_{par} > 1$, leading to the following requirement:

$$\frac{g_m}{C_{par}} \times \frac{2L}{R_{ind}+R_{gate}} > 1. \quad (3)$$

While the first term on the left represents a dependence related to TFT f_T, the second term depends strongly on the patterned inductor (with some dependence on the TFT through R_{gate}). Thus, the ability to pattern high-quality inductors can be exploited to overcome the low-performance of the TFTs. With planar inductors of radius of 3 cm, the measured $2L/(R_{ind}+R_{gate})$ is 7.5 μH/Ω. The fabricated TFTs ($W/L = 3600\ \mu$m$/6\ \mu$m), operating at a solar-module voltage (V_{op}) of 25 V, have a measured g_m/C_{par} of 7.3×10^6 rad/s. This yields a resonant frequency of 700 kHz. The resulting value of $g_m \times R_{par}$ is 54.8, allowing oscillations to be robustly achieved with an amplitude of 12 V. An additional benefit of the free-running LC-oscillator power inverter, compared to the switching topology, is that no additional control circuitry is required, whose overhead can be substantial when implemented with TFTs. Thus, the inverter achieves a power-transfer efficiency of 30% while enabling an output power of 22 mW, which is well beyond the system needs.

2) CMOS Power-Management Circuits: The primary blocks of the power-management subsystem in the CMOS domain are as follows: a full-wave diode rectifier, whose DC output is stored on the storage capacitor C_{STO}; a low-level voltage monitor; an overvoltage-protection circuit; a bias-level generator; three switch-capacitor DC-DC converters with local output-level monitors for voltage regulation; and a clock generator for the DC-DC converters. The blocks enable the generation of three regulated voltage supplies (2.4 V, 1.2 V, 0.6 V) upon assertion of a REQ signal (can be provided by a microcontroller).

The 12 V amplitude from the LAE power inverter is stepped down by a factor of 1/3 through the turns ratio of the inductive interface. The voltage stored on C_{STO} (i.e., V_{STO}) is regulated nominally between 3.2–3.6 V via the low-level voltage monitor and overvoltage protection circuits. Figs. 7 and 8 show these circuits and their simulated waveforms. The low-level voltage monitor implements hysteretic control of ENb using a comparator. ENb both controls a PMOS switch, which shifts the comparator's input voltage to implement hysteresis, and enables the DC-DC clock generator; as a result, the DC-DC converters can begin drawing charge from C_{STO}. The overvoltage-protection circuit provides protection against excessive charging of C_{STO} beyond the nominal 3.6 V limit of the CMOS transistors by controlling a shunting current through $R_{protect}$. The shunting current effectively modulates a reflected impedance appearing in parallel with the resonant tank of the thin-film power inverter. This substantially dampens the resulting oscillations. As a result, V_{STO} is regulated both by shunting current off C_{STO} and by mitigating further charging on C_{STO}. The biasing and reference required for all of the power-management circuits is generated via on-chip diode structures, as illustrated in Fig. 9.

Fig. 10(a) shows the switch-capacitor structure of the three DC-DC converters along with their voltage-level monitors at each output, and Fig. 10(b) shows the relaxation-oscillator clock generator. The DC-DC converters implement 3/4, 1/2, and 1/4 voltage conversion, respectively. The voltage-level monitors provide voltage regulation at the desired levels by gating the clock to generate each converter's ϕ1/2 switching signals; this is done through hysteretic control enabled by comparators having corresponding input reference voltages. When the desired output levels are reached, each voltage-level monitor asserts a ready signal (RDY1/2/3); these are then NANDed to generate ACKb, indicating the supplies are available for use by the IC.

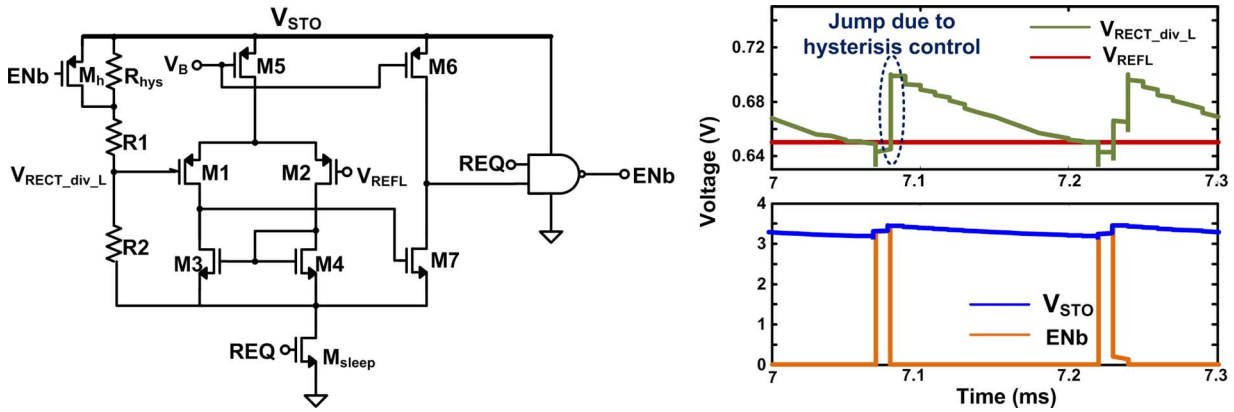


Fig. 7. Circuit details of low-level voltage monitor and its simulated waveforms.

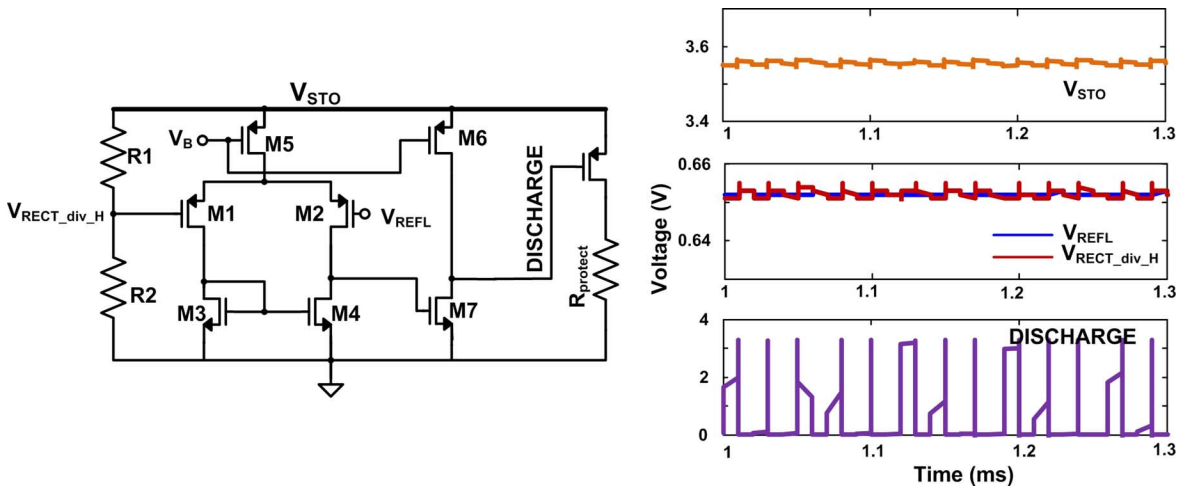


Fig. 8. Details of the over-voltage protection circuit and its simulated waveforms.

B. Sensing Subsystem

Fig. 11 shows the architectural blocks of the sensing subsystem. The LAE domain consists of a thin-film sensor array formed by TFTs, sensor-signal readout and modulation circuitry, and sensor access-control circuitry. The CMOS domain consists of sensor-signal acquisition and digitization circuitry and sequential sensor-readout control circuitry. There are two important aspects of the architecture. First, it enables interfacing with TFT-based sensors. TFTs, having shown rich physical responses, form the basis for a wide range of demonstrated sensors ([14], etc.). Such an architecture thus has the potential to address a range of LAE sensing applications. Second, it minimizes the number of interface signals between the LAE and CMOS domains. This substantially enhances system scalability while enabling measurements over a large number of LAE sensors. As described below, this is achieved via TFT-based access-control circuits for readout and sensor selection.

1) LAE Sensing Circuits: Strain sensing is realized through the mobility response of a-Si TFTs. TFTs ideally exhibit a linear mobility relationship with strain, as shown by the measurements from fabricated TFTs plotted in Fig. 12. Consequently, the TFT current can be used to derive a gauge factor $(\Delta I_{DS}/I_{DS})/(\Delta L/L)$, which is measured to be approximately 7.5 (where I_{DS} is the TFT drain-source current and L is the length of the TFT channel along the direction of strain). Compared with resistive strain sensors, which have a gauge factor of $\sim$2 and are widely used, TFTs give greater response [15].

A challenge, generally, with TFT-based sensors is that the output signal, which is typically their current, is DC. Readout over a non-contact interface therefore requires AC modulation. This is achieved using the TFT-based differential Gilbert cell shown in Fig. 13. The benefit of a differential structure is that only the strain-response of the TFTs, and not their DC biasing current, appears at the output; this can be seen in the simulation waveforms shown for different simulated values of strain-induced ΔI_{DS}. However, differential readout requires the use of a reference TFT that is not subject to strain. This is achieved by patterning a TFT whose channel orientation is orthogonal to that of the sensing TFT. Similar approaches are used with resistive sensors for uniaxial strain sensing; multiple-axis sensing can then be achieved by patterning various orientations of the reference and sensing devices. Individual sensors in the subarray are selected by controlling a corresponding access switch, as shown in Fig. 13; the generation of the access-control signals (EN[i]) for sequential sensor readout is described below. Once AC modulated, the sensor signal is coupled to the CMOS IC via a capacitive interface. Capacitive, rather than inductive, coupling is

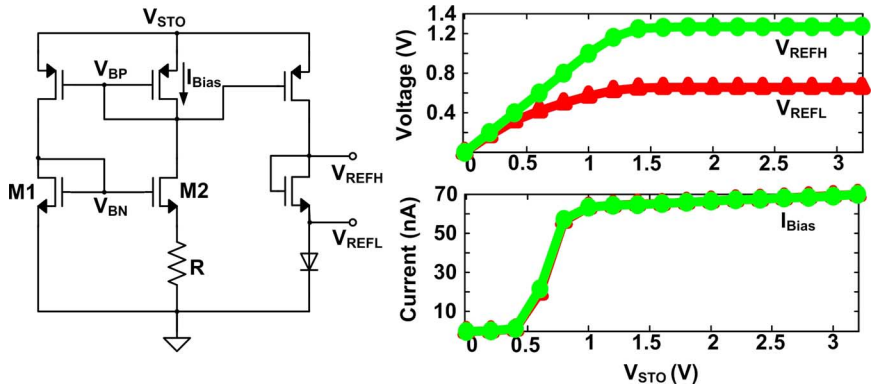


Fig. 9. Sample biasing and reference-generation circuit with DC sweep on V_{STO} showing the generation of biasing levels (V_{REFH}/V_{REFL}) for the low-level voltage monitor, over-voltage protection circuit, DC-DC converters, and clock generator.

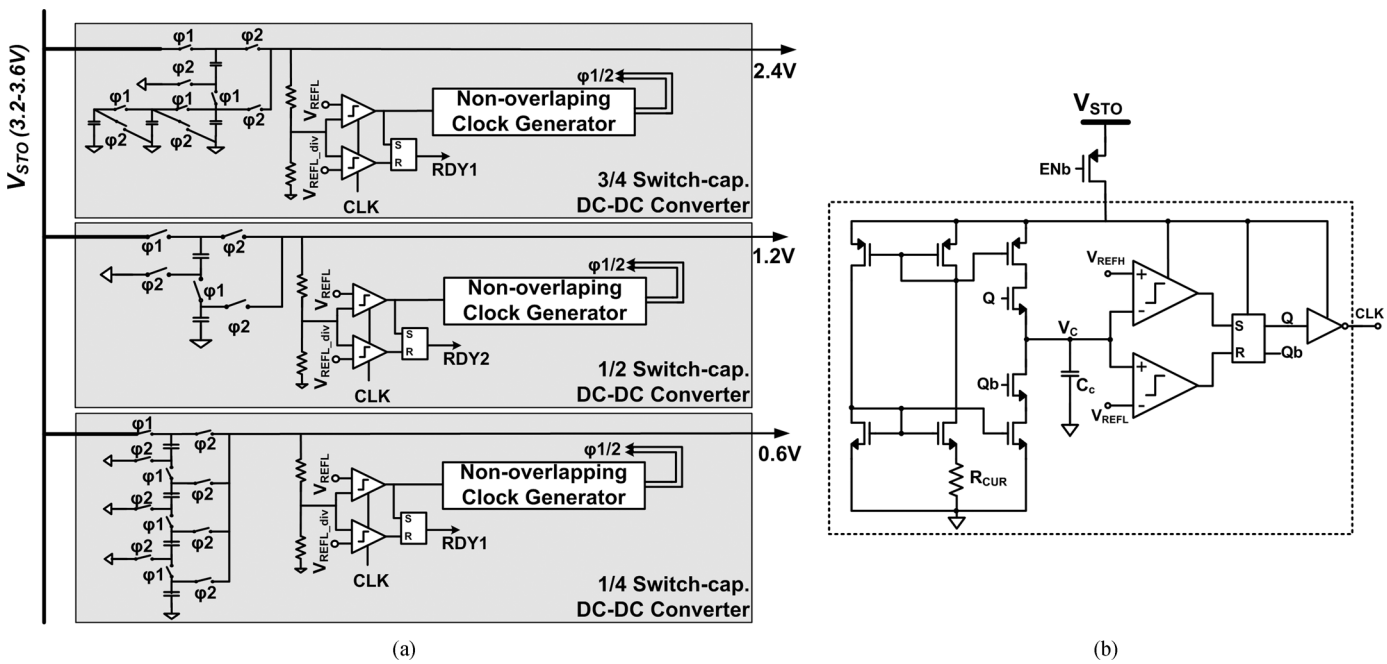


Fig. 10. (a) Details of three DC/DC converters for 0.6 V, 1.2 V and 2.4 V supplies. (b) Relaxation oscillator circuit for DC/DC converter clock generation.

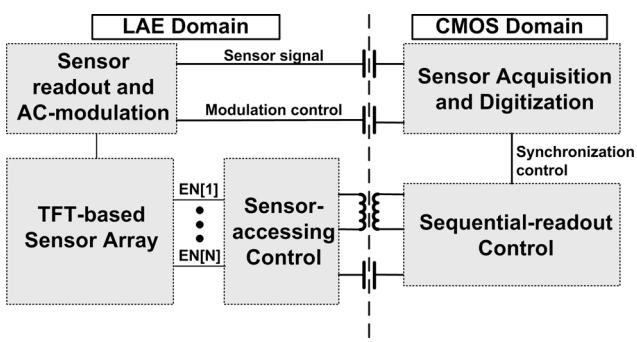


Fig. 11. Architectural blocks of the sensing subsystem.

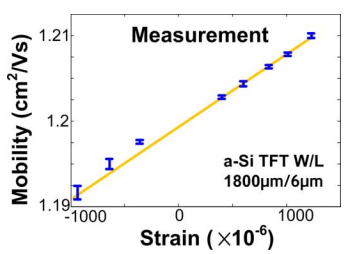


Fig. 12. Mobility response of TFT-based strain sensors.

chosen since the modulation frequency for the Gilbert cell is limited by the TFT f_T. A modulation frequency of 100 kHz is thus used, and this is provided by the CMOS IC (to enable the synchronous acquisition described below) also via a capacitive interface. The resistive loads of the Gilbert cell are realized using thin-film resistors implemented via n^+-doped a-Si deposition; this yields a reproducible resistivity of 30 $M\Omega/sq$.

For sensor-accessing control, two options are provided. In order to minimize the interfacing signals required to the CMOS IC, both options use the scanning circuit shown in Fig. 14. The scanning circuit generates all the sensor EN[i] signals by using just four input control signals. A key challenge in the scanning circuit is ensuring full-swing voltage levels in the absence

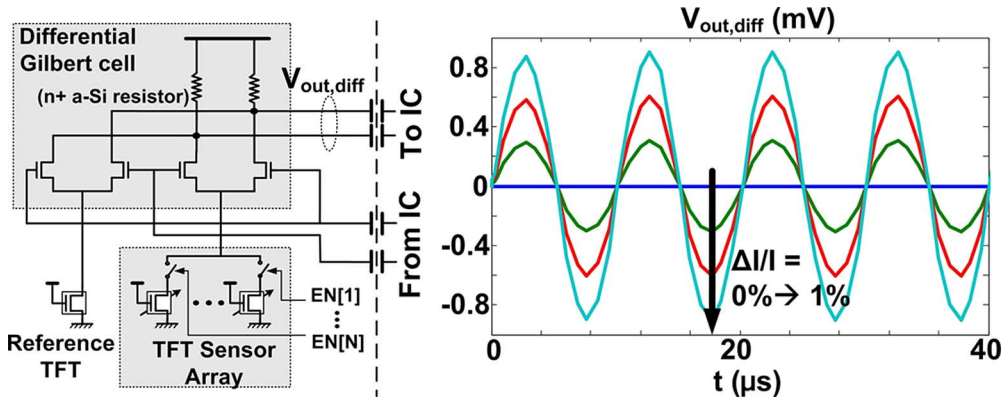


Fig. 13. Thin-film differential Gilbert cell with simulations showing the output voltage generated due to different $\Delta I_{DS}/I_{DS}$ from the TFT sensors.

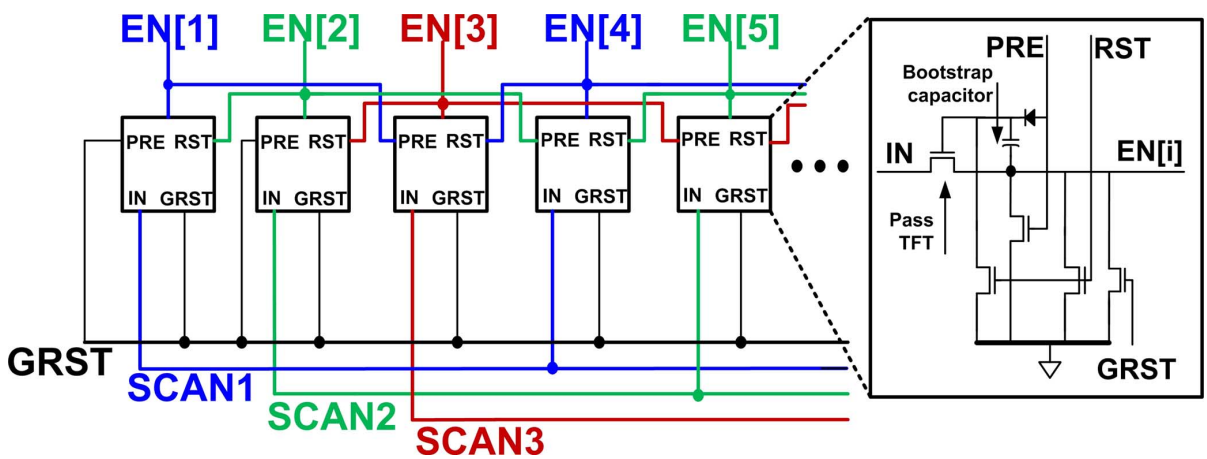


Fig. 14. Thin-film scanning circuit for generating sequential TFT-sensor enable signals (EN[i]) using four input control signals (GRST, SCAN1–3).

of PMOS transistors. This is achieved in the circuit shown [7] via capacitive bootstrapping applied to a pass-transistor. Three-phase control, implemented by SCAN1–3, is thus used to precharge, drive, and reset the bootstrap capacitor (precharging is achieved via a thin-film a-Si Schottky diode); an additional interface signal (GRST) is require for initial global resetting.

There are two options for generating the three-phase SCAN1–3 signals: 1) IC-based control, which permits precise timing and configurability; and 2) LAE-based self control, which requires less system power. IC-based control uses AC-modulated versions of the digital control signals from the CMOS domain to the LAE domain. A key challenge with this approach is that the IC can operate at up to 2.4 V but the LAE scanning circuits require over 6 V for robust operation. Consequently, inductive interfaces are used to enable voltage step up. To minimize power, the inductive interfaces operate at resonance, wherein high resonant frequencies are preferred for minimizing inductor losses. The achievable frequency is limited by the capacitance of a subsequent thin-film rectifier, required to demodulate the digital control signals. The full-wave rectifier shown in Fig. 15(a) utilizes nanocrystalline-silicon (nc-Si) Schottky-barrier diodes rather than a-Si diodes (as in [7]). These are processed at 180°C, as shown in Fig. 15(b), and give over 1000× higher current density than a-Si diodes [16], thereby enabling smaller structures for reduced capacitance. 0.09 mm^2 diodes are thus used, giving a capacitance of 36 pF (compared to 1 mm^2 diodes with 130 pF capacitance for the a-Si structures in [7]). The resulting interface frequency is 3 MHz with 78 μH inductors, giving a quality factor of 113.

LAE-based control is achieved using the three-phase non-overlapping clock generator shown in Fig. 16. The circuit consists of three ring oscillators implemented by resistively-loaded inverter stages (resistors are implemented via n$^+$-doped a-Si). The ring-oscillator outputs are coupled using an effective three-input NOR gate to achieve non-overlapping SCAN1–3 signals (note, GRST is provided by the IC through an inductive interface as above). Due to the use of free-running oscillators, the duration of each signal is imprecisely controlled. However, the benefit is that coupling to the CMOS IC does not require voltage step up or AC-modulation, thereby reducing power. Rather, the SCAN1–3 signals can be provided directly to the CMOS IC via capacitive coupling; as described below, the IC then performs sequential sensor acquisition by detecting the SCAN1–3 edges, which can be done robustly thanks to the high-speed CMOS transistors. As described in Section IV-B, the power consumption of the IC-based control is substantial due to the need for voltage step up. Additionally, since the power is drawn from a CMOS supply, the losses of the power-management circuit (e.g., power inverter) are also a factor. LAE-based control thus has substantial potential to save system power.

2) CMOS Sensing Circuits: The primary blocks of the sensing subsystem in the CMOS IC are a synchronous G_M-C

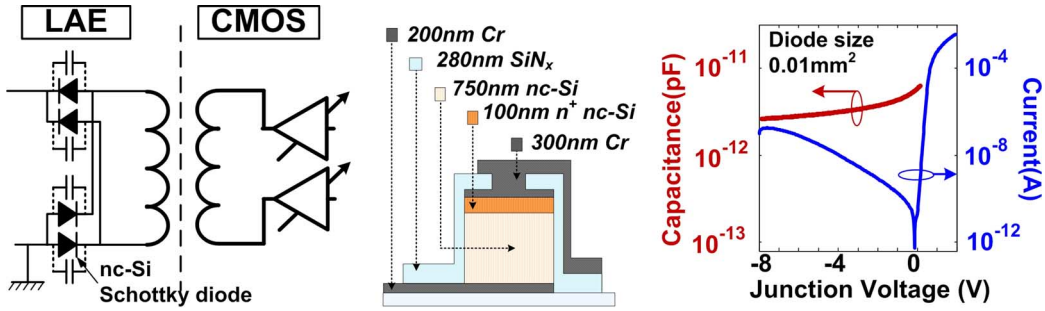


Fig. 15. IC-based sensor-accessing control uses (a) a thin-film full-wave rectifier based on Schottky diodes for demodulaton of IC control signals, and (b) nano-crystalline silicon (nc-Si) diodes yield 1000 × higher current density (compared to a-Si diodes), enabling smaller devices and reduced resonant capacitance for higher frequency of the inductive interfaces.

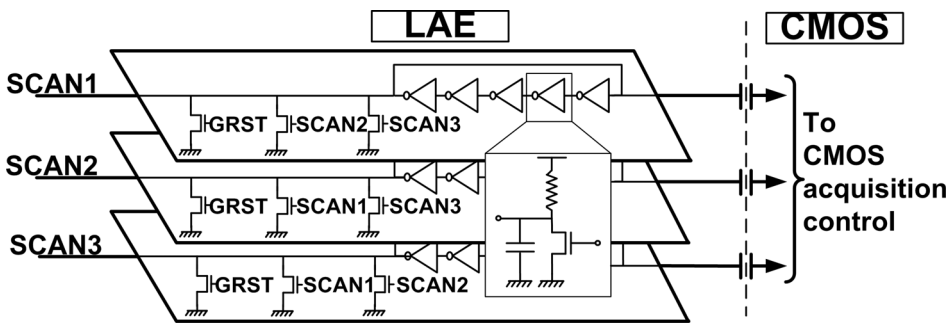


Fig. 16. LAE-based three-phase control is achieved using NOR-gate coupled TFT oscillators and interfacing with IC is achieved capacitively to enable edge detection for synchronization.

integrating ADC for sensor acquisition and digitization (along with sensor-modulation signal generator) and a sequential-readout control block. Digital control logic is also included for control and configuration.

The synchronous G_M-C integrating ADC is shown in Fig. 17. Amplification and demodulation of the sensor signal is performed by a G_M stage. With demodulation performed at the output node as shown, the subsystem effectively implements chopper stabilization for sensor acquisition (with input modulation performed by the LAE Gilbert cell). Consequently, offsets and 1/f noise are mitigated. The demodulated G_M current is then fed to an op-amp integrator for a fixed duration, and 10-b digitization is achieved by counting the clock-cycles required to discharge the integration capacitor via a constant current source. For user-initiated calibration of offsets in the entire sensor subsystem (including the LAE sensors and circuits), a 9-b current DAC is included at the G_M-stage output. To reduce the power consumption of the op-amp, output dominant-pole compensation can be used thanks to the low-bandwidth requirements of the op-amp. The sensor-modulation signal (for the LAE Gilbert cell) is generated via a digital delay line followed by a tunable-drive Class-D power amplifier (PA). The digital delay line enables alignment of pulses for synchronous sensor acquisition.

The sequential-readout control block is used to generate GRST and generate/detect SCAN1–3 signals for sensor-accessing control. Fig. 18(a) shows the circuit for IC-based control. A self-circulating shift register is used with an output modulator, running at the inductor-interface frequency. A

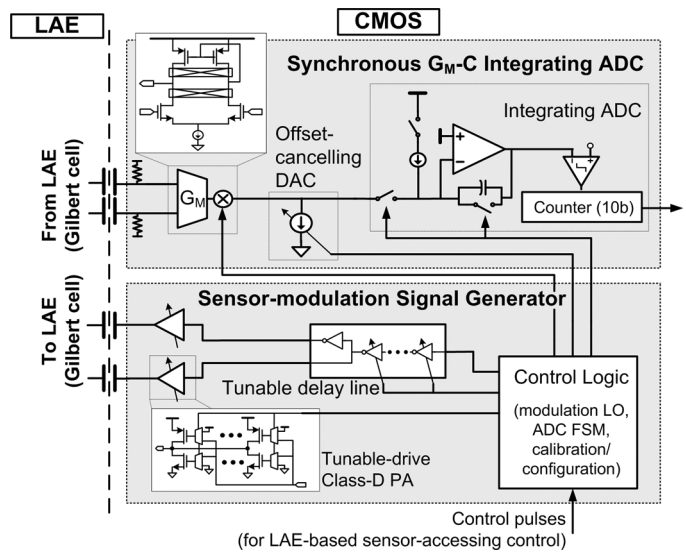


Fig. 17. Details of the CMOS G_M-C integrating ADC and sensor-modulation signal generator.

variable-drive Class-C PA is then used to drive the interface inductors. Though all other CMOS circuits of the sensing subsystem operate from the 1.2 V supply, the PAs operate from the 2.4 V supply in order to minimize the voltage step-up required in the inductive interface; this mitigates inductor losses by easing the turns ratio, thereby enabling thicker traces with lower resistance. Fig. 18(b) shows the circuit for LAE-based control. Continuous-time comparators, followed by delay

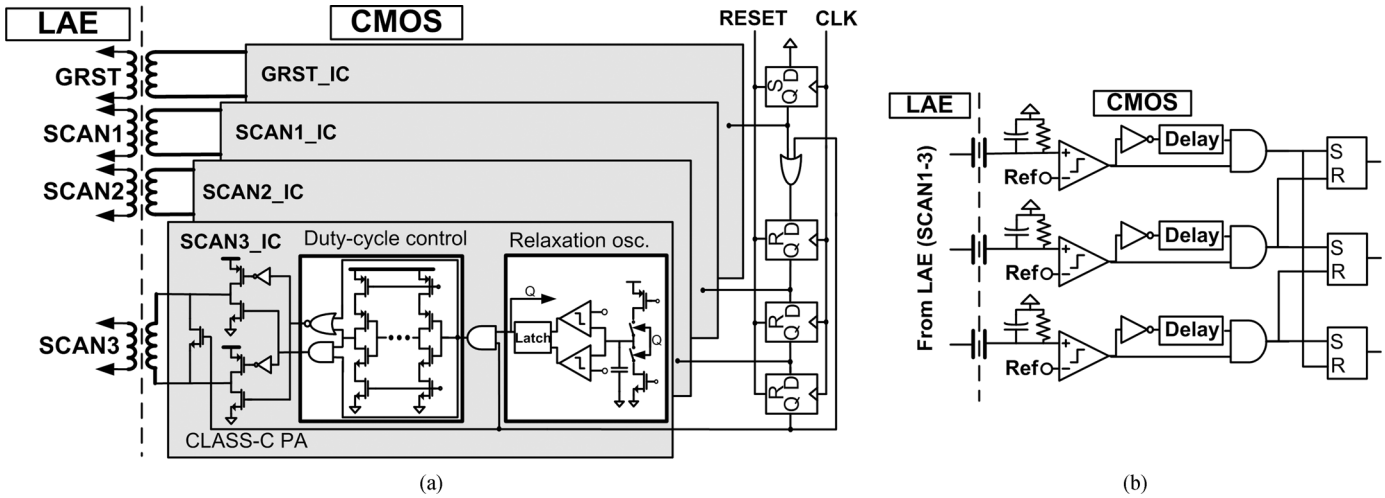


Fig. 18. Sequential readout control block for (a) IC-based sensor-accessing control and (b) LAE-based sensor-accessing control.

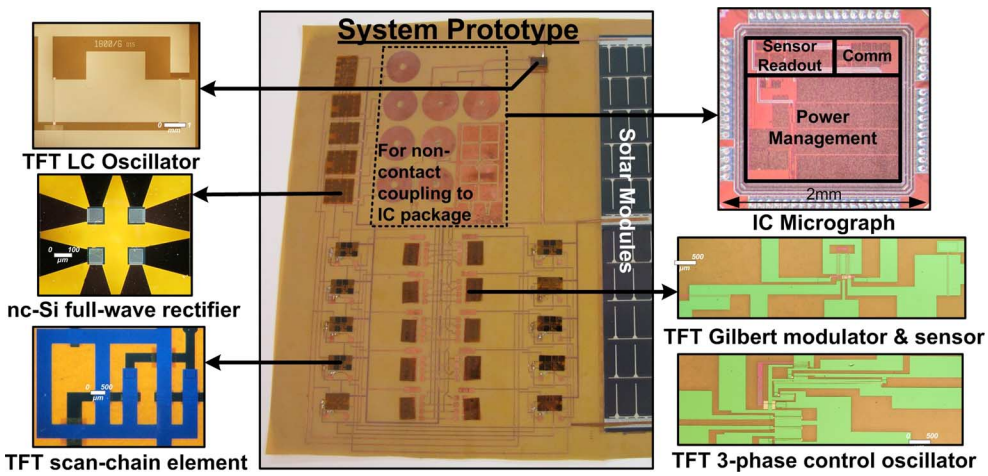


Fig. 19. System prototype, consisting of CMOS IC fabricated in a 130 nm process from IBM and LAE circuits fabricated in house on 50-μm-thick polyimide.

lines, are used to generate digital pulses upon detection of the SCAN1–3 edges. The pulses are latched and provided to the acquisition-circuit control logic for sequential sensor readout.

C. Communication Subsystem

The communication subsystem is based on the architecture presented in [7]. The LAE domain consists of metal interconnects that can be long ($\sim$10 m), enabling low-energy communication among ICs distributed over the large-area sheet; since the ICs perform sensor data-acquisition, this enables data aggregation over the LAE sheet. The CMOS domain consists of an on-off-keying (OOK) transceiver [7]. To minimize the transmit power, the carrier-frequency, set by a digitally controller oscillator (DCO), is tuned via a calibration block to the resonant point of the LAE interconnect. In this design, the calibration-block circuitry (ADC, digital control, etc.) is integrated within the transceiver. The nominal carrier frequency is 15 MHz, which permits efficient use of inductive interfaces. The transmit and receive signal levels can thus be optimized; transmit-signal step-down is employed to minimize resistive losses in the LAE interconnects and receive-signal step-up is employed to maximize receive SNR [7].

IV. System Prototype and Measurement Results

Fig. 19 shows the system prototype. The CMOS IC is fabricated using a 130 nm process from IBM, and the LAE components are fabricated in house on 50-μm-thick polyimide foil. The TFTs are based on partially hydrogenated a-Si (a-Si:H), processed at 180°C in a plasma-enhanced chemical-vapor deposition system (PECVD) [9]. The LAE interconnect as well as the interface inductors and capacitors are patterned with 10-μm-thick copper. An overall performance summary of the system is given in Table I, and detailed characterization results are presented in the subsections below. Measurements show that fully-self-powered operation of the entire system is easily achieved with the 300 cm^2 solar modules adopted.

Fig. 20 shows the oscilloscope-captured waveforms for the entire system, including power management, sensing, and communication. For the power-management subsystem, when power is available from the a-Si solar module, the thin-film power inverter turns on and converts the DC power to AC for wireless power delivery to the CMOS IC. The IC's storage-capacitor C_{STO} is charged through a rectifier, causing its voltage V_{STO} to rise. When the REQ signal is asserted, the three DC-DC converters are enabled, eventually generating the

TABLE I
PERFORMANCE SUMMARY OF SYSTEM PROTOTYPE

Performance summary			
Technology			
LAE		a-Si on 50μm polyimide @ 180 °C	
CMOS IC		130nm CMOS	
Power Management Subsystem			
TFT Power Inverter η	30%	DC-DC output voltages	0.6V,1.2V,2.4V
Solar Module Size	300cm²	Overall DC-DC converter η	80.5%
Sensing Subsystem (for TFT sensing)			
Max. Readout Noise	22.9μStrain$_{RMS}$	Max. Readout Non-linearity	28.6μStrain
Max. Energy/meas.	434nJ	Max. Measurement/sec.	500
Communication Subsystem			
Tx Energy (@7.5)	14.6pJ/bit	Max. Data Rate	2Mb/s
Rx Energy (@7.5)	4.3pJ/bit	Self-calibration Loop Energy	17μJ

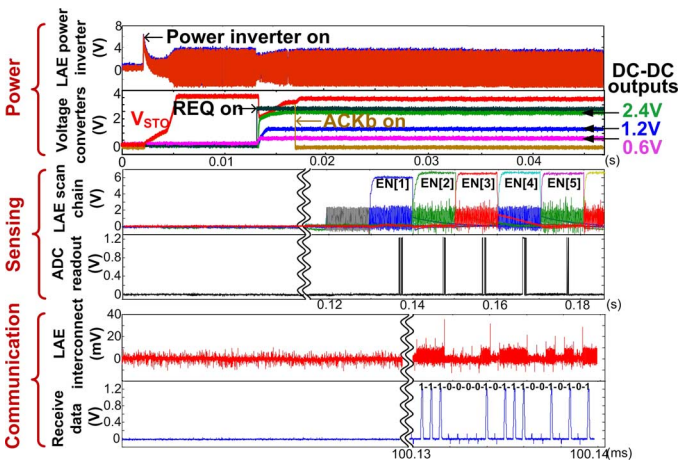
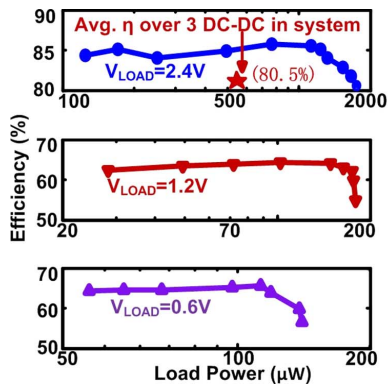


Fig. 20. Measured waveforms for system prototype from oscilloscope capture.



LAE performance	
Solar module size	300 cm²
TFT power inverter η_{max}	30%
TFT power inverter freq.	0.7 ~ 2 MHz
CMOS IC performance	
DC-DC output voltages	0.6V, 1.2V, 2.4V
Overall DC-DC converters η	80.5%
Standby power	1.6μW

Fig. 21. Measurement results for the power-management subsystem.

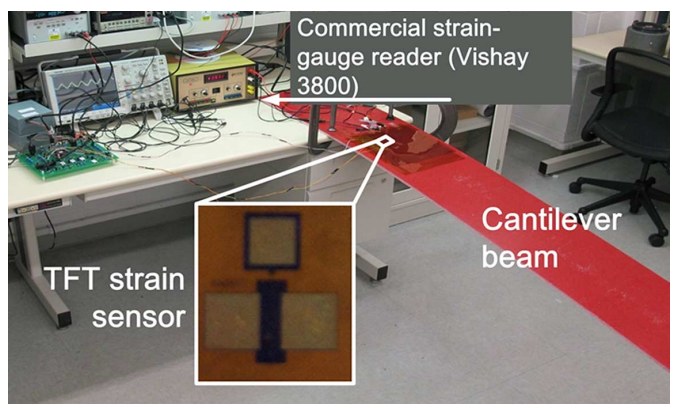


Fig. 22. Testing setup used in the lab for the sensing subsystem.

required supply voltages, at which point the ACK signal is asserted. For the sensing subsystem, AC-modulated three-phase control signals are generated from the IC with a swing of 2.4 V; these signals are stepped up to 6.5 V in the LAE domain and rectified to generate the SCAN1–3 signals, which in turn generate the sequential sensor enable signals (EN[i]) via the TFT-based scanning circuit. Sequential readout through the CMOS G_M-C integrating ADC is performed for the individual sensors, and the digitized signal is output serially as shown. For the communication subsystem, the transmit data on the LAE interconnect is shown (4 mV amplitude) along with the receive data from the clocked comparator.

A. Power-Management Subsystem Testing

Fig. 21 shows measurement results for the power-management subsystem. The 300 cm^2 a-Si solar module generates 25 V to the thin-film power inverter. The measured combined efficiency of power inverter and inductive link (with 100 μm coupling separation) is 30% using 3 cm-radius coupling inductors. The maximum output power is 22 mW, well beyond the system requirement.

In sleep mode (REQ is low), the CMOS-IC power management system consumes 0.5 μA from V_{STO}. This is consumed by the bias and reference generator and over-voltage protection circuits. While in active mode (REQ is high) without any load on the three DC-DC converters, the CMOS-IC power management system consumes 10 μA from V_{STO}. This includes the circuitry in sleep mode plus low-level monitor, clock generator and DC-DC control circuitry. The DC-DC converters generate 0.6 V, 1.2 V and 2.4 V DC supplies for use by the other subsystems. The total size of the on-chip dual-MIM capacitor arrays used are 400 pF, 120 pF and 2700 pF, occupying a total area of 0.75 mm^2. The targeted power levels of three supplies are 140 μW, 180 μW, and 1.5 mW, respectively. The average power-conversion efficient of the three DC-DC converters is 80.5%, with the majority of the power drawn from the 2.4 V supply.

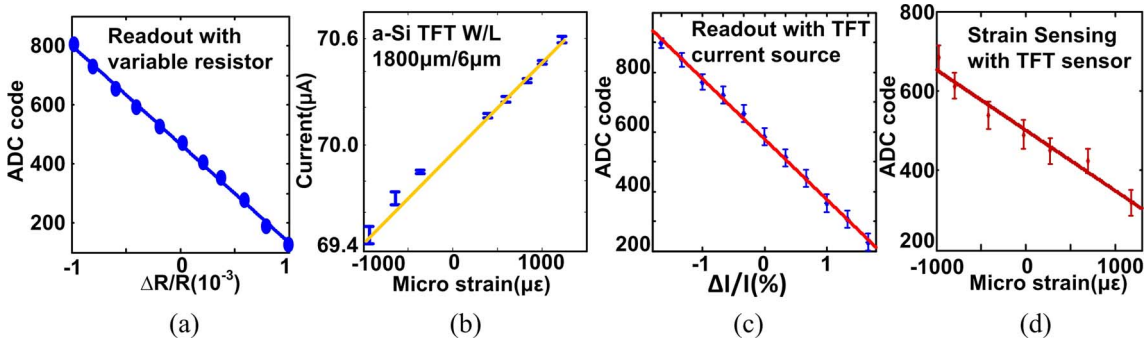


Fig. 23. Sensor subsystem response showing (a) CMOS acquisition characterization with a variable resistor driven by the CMOS-generated modulation signal, (b) isolated strain response of TFT-sensor current, (c) isolated readout performance of acquisition circuits obtained by using a calibrated TFT current source at the tail node of the LAE Gilbert cell, and (d) overall strain response of the system using TFT sensors.

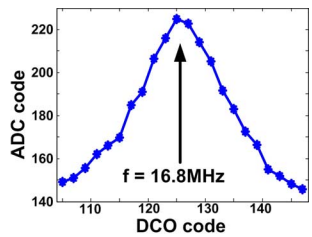
B. Sensing Subsystem Testing

To characterize the sensing subsystem, tests were performed using a calibrated current source, resistive strain gauges, and TFT-based strain sensors. Fig. 22 shows the testing setup used in the lab for the sensing subsystem. TFT-based strain sensors were bonded to a 180 cm cantilever beam which was loaded with known weights. Reference strain gauges (resistive), measured using a commercial readout system (Vishay 3800), were also bonded for comparison. Before testing the complete system, the CMOS acquisition circuits, the TFT-based strain sensors, and the integrated LAE-CMOS readout circuits (i.e., TFT Gilbert cell with CMOS acquisition circuits) were each characterized in isolation. To characterize the CMOS acquisition circuits, a variable resistor driven by the CMOS-generated modulation signal was used; Fig. 23(a) shows the response, with maximum nonlinearity of 28.6 μStrain and noise level of 22.9 $\mu\text{Strain}_{\text{RMS}}$. To characterize the TFT strain sensor, the TFT current was read using a transimpedance amplifier; Fig. 23(b) shows the response, with maximum nonlinearity of 140 μStrain. To characterize the the integrated LAE-CMOS readout circuits, a variable TFT current source was used at the Gilbert-cell tail node; Fig. 23(c) shows the response, with maximum nonlinearity of 45 μStrain and noise level of 106 $\mu\text{Strain}_{\text{RMS}}$. Fig. 23(d) shows the strain-readout performance of the complete system using TFT strain sensors and LAE-CMOS readout circuits; the maximum nonlinearity and noise level are 180 μStrain and 141 $\mu\text{Strain}_{\text{RMS}}$ respectively, which meet the requirements for damage detection in SHM applications [2]. The increased nonlinearity and noise are due to low-frequency threshold-voltage noise in the a-Si TFTs.

The measured power consumptions of each sub-block is as follows. 45 μW is consumed by the sensor-modulation signal generator, including the relaxation oscillator, delay line, and PAs. 29 μW is consumed by the acquisition circuits, including the G_M stage and ADC. 143 μW is consumed by the sequential readout control circuits when IC-based sensor-accessing control is used, while 112 μW is consumed if LAE-based control is used (considering the efficiency of the power-management subsystem, IC-based control thus consumes 4.2$\times$ more power from the LAE energy harvester). The maximum access speed is 500 Hz, limited by the operation of the LAE scan chain. The resulting IC energy/measurement is 148 nJ for acquisition and 286 nJ for IC-based sensor-access control.

Tx/Rx energy (@7.5m)	14.6pJ/bit 4.3pJ/bit
Max.data rate	2Mb/s
BER	$< 10^{-5}$
Self-cali. loop energy	17μJ

(a)



(b)

Fig. 24. Communication subsystem measurements, showing (a) the performance summary [7], and (b) calibration-loop sweep used to set the DCO frequency to the interconnect resonant point.

C. Communication Subsystem Testing

To characterize the communication subsystem, long-range LAE interconnects (up to 7.5 m) are used for communication between a transmitting IC and a receiving IC [7]. Fig. 24(a) shows the measured performance of the transceiver. At a distance of 7.5 m, the transmitter consumes 14.6 pJ/bit while the receiver consumes 4.3 pJ/bit, with a BER $< 10^{-5}$. The carrier-frequency calibration loop consumes 17 μJ. Fig. 24(b) shows the digitized receive envelop during the calibration phase. The resonant peak is observed at a frequency of 16.8 MHz, and the DCO frequency is set accordingly.

V. Conclusions

This paper presents the architecture and design of a scalable strain-sensing system for structural-health monitoring applications. The system combines LAE and CMOS technologies to leverage their respective strengths within power-management, sensing, and communication subsystems. To allow the functionality of each subsystem to be optimally distributed between the two technologies, non-contact interfaces based on inductive and capacitive coupling are employed. These substantially improve system scalability by avoiding metallurgical bonds at the interfaces of the two technologies.

The power-management subsystem enables full self-powered operation through a solar-module and power-conversion architecture based on TFT and CMOS circuits. The sensing

subsystem enables sequential acquisition and digitization over an array of TFT-based strain sensors. By employing circuits that enable readout of TFT-based sensors, the architecture has the potential to generalize to applications based on the broad range of different TFT sensors that have been demonstrated. The communication subsystem enables low-energy data aggregation over CMOS ICs that are distributed over a large-area sheet spanning several meters.

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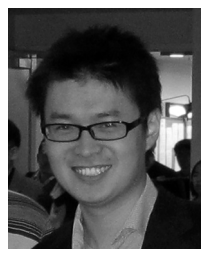

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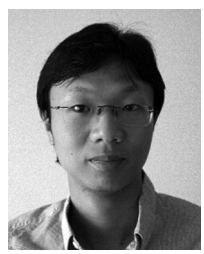

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